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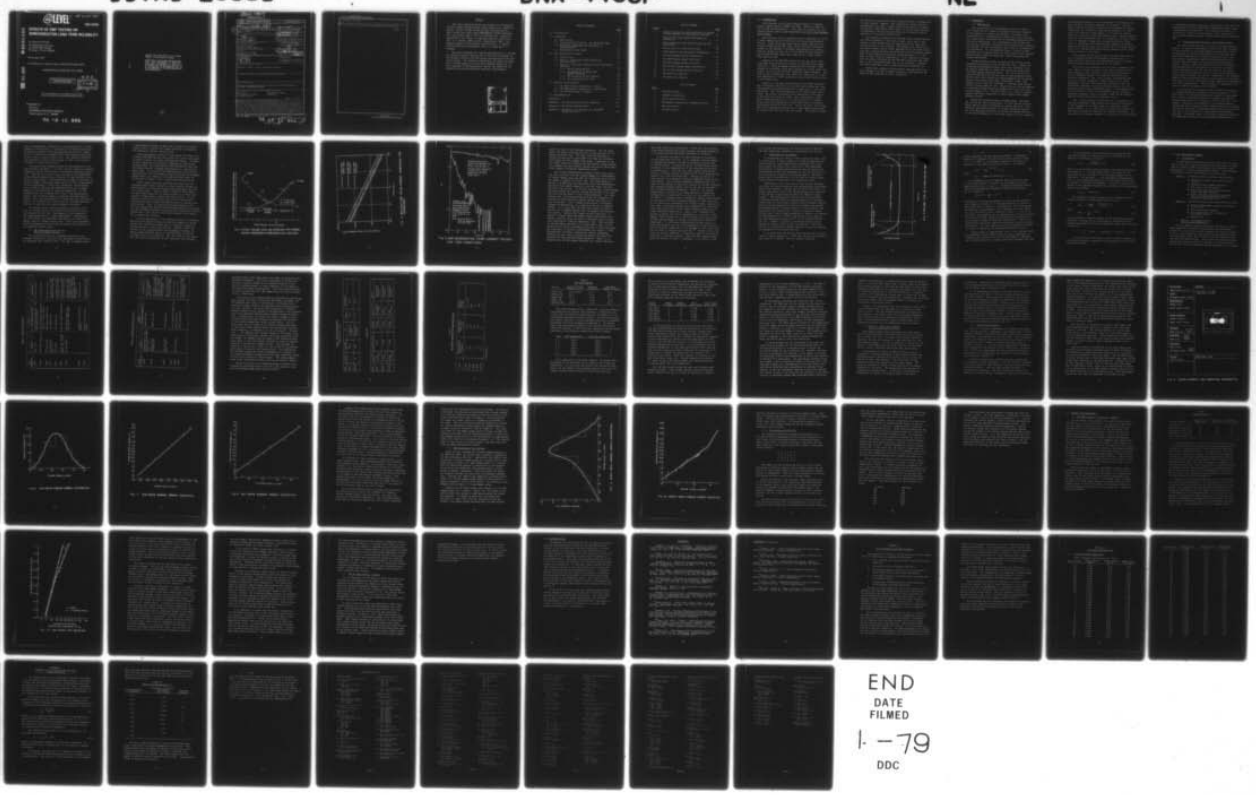

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EFFECTS OF EMP TESTING ON SEMICONDUCTOR LONG TERM RELIABILITY

Dr. Sherwin R. Kahn

IIT Research Institute
10 West 35th Street
Chicago, Illinois 60616

November 1977

Final Report for Period 1 April 1976—31 October 1977

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The objective of this research effort has been to determine the long-term reliability effects of pre-stressing semiconductor devices with EMP-like transients. This study was conducted by subjecting large sample lots (~100 per lot) of the JAN 2N918 transistor and the JAN-TX IN914 diode to these electrical transients at a large and a small fraction of the nominal Wunsch damage level for each device. These pre-stressed devices together with an un-stressed control lot were then life tested at a junction temperature of 300°C for a continuous 1280 hour period. The effects of EMP pre-stressing on the reliability →over.

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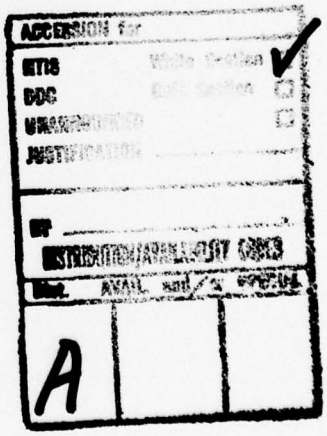
20. ABSTRACT (Continued)

of these devices were then assessed by comparing the observed failure rates of the various sample lots under these accelerated life test conditions.

PREFACE

This Final Technical Report was prepared by IIT Research Institute under Defense Nuclear Agency Contract No. DNA001-76-C-0243, "Effects of EMP Testing on Long Term Reliability," RDT & E RMSS Code B3230 76464 R99QAXEB09761 H2590D performed over the period 1 April 1976 to 31 October 1977. Technical monitoring of the contract at DNA was under the direction of Capt. W. D. Wilson, RAEV, and Mr. George Baker, RAEV. The program manager at IIT Research Institute was T. A. Martin, and the principle investigators were S. R. Kahn and V. C. Formanek.

The author expresses his sincere appreciation to J. Dittman for technical support services and to his other colleagues at IIT Research Institute for their many contributions to the work reported here. The technical consultation and advice provided by Dr. Donald Wunsch of the Air Force Weapons Laboratory, Mr. Dave Alexander of BDM Corporation, and Mr. Roy Walker of the Reliability Analysis Center are especially acknowledged.



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1.0 INTRODUCTION

This document is the Final Technical Report for Defense Nuclear Agency Contract DNA001-76-C-0243, "Effects of EMP Testing on Long Term Reliability." This work was sponsored by the Defense Nuclear Agency under RDT&E RMSS Code B3230 76464 R99QAXEB 09761 H2590D.

The objective of this study has been to determine the effect of EMP stressing on the reliability of selected semiconductor devices. Three transistor types and two diode types were subjected to high and low EMP stress levels and their reliability studied by the methods of thermally accelerated life testing. From the results of this test the JAN 2N918 bipolar transistor and the JAN TX 1N914 diode were selected for a large sample, long term life test.

Samples of the JAN 2N918 transistor and the JAN TX 1N914 diode were pulse stressed to failure to determine their damage statistics. Using the damage thresholds thus obtained, large samples of both device types were stressed at a large (0.93) and a small (0.1) fraction of their respective damage energies. The devices thus stressed were life tested for 1280 hours at a junction temperature of 300°C along with an unstressed control group of each device type.

Analysis of the data obtained for the JAN 2N918 indicates that the devices subjected to a low EMP stress suffer more late time failures than those stressed at a high level or those left unstressed. The life distributions of all three groups (high stress, low stress, and control) are substantially the same up to 500 hours of testing at 300°C. This corresponds to 3650 device operating years (3.2×10^7 device hours) at a nominal service junction temperature of 100°C based upon an estimated accelerating factor of 6.36×10^4. After this time, the failure rate of the population stressed at 0.1 mean damage energy shows an increase over the other two test groups. The slight increase

in failure rate beyond 3650 device operating years is unimportant for most systems. However, this increase may warrant serious consideration for large, complex electronic systems or networks containing a sufficiently large number of devices where hundreds of thousands of device operating hours can be realized before completion of the normal service life.

The increased reliability of the high level stressed devices over those stressed at a low level is most likely due to the removal of weak devices from the population by the high level stressing prior to life testing. Such devices, not removed by a low stress screen, may be subtly degraded by the low level stress such that a deviation from the unstressed life distribution occurs after a very long period of device operating hours ($> 3 \times 10^7$ hours at 100°C junction temperature). It is important to stress that the results obtained for the JAN 2N918 transistor may apply only to this particular device due to its structure. Moreover, the results may apply only to this particular production lot.

Insufficient numbers of failures were observed during the life testing of the JAN TX 1N914 to draw any conclusions on the effect of EMP stressing on their reliability.

2.0 BACKGROUND

2.1 EMP Testing

The susceptibility of semiconductor devices to EMP is well recognized and a number of programs have been conducted or are underway to resolve this problem. Typically, this susceptibility is investigated by conducting tests-to-failure on a large number of devices and by developing supporting theoretical failure models. As a consequence, some thought has been given to EMP pulse screening tests during device production to eliminate the more susceptible units prior to incorporation into equipments. At the equipment level, a variety of EMP exposures can be expected over the entire life of the equipment during various stages of production, system acceptance and routine maintenance.

In EMP-hardened systems the need for EMP testing arises throughout many phases of the system life cycle. During the system design/development phase, piece part screening tests are usually conducted to verify that the device meets established EMP damage threshold levels. This is of special concern when EMP-sensitive devices such as semiconductors and/or similar solid state devices are being designed into the system. Because these devices are highly susceptible to EMP, 100% inspection tests have been proposed to eliminate weak devices within a given production lot. These tests are also recommended to establish minimum design requirements for the circuit protection elements (i.e., filters, TPD's, etc.) used to suppress expected EMP input transients to these devices below damage producing levels.

During the production and/or assembly phase, additional EMP testing has also been proposed. In such testing, semiconductor devices could be subjected to several EMP tests. The magnitude and characteristics of the EMP transients applied can vary depending on whether the pulses are applied directly to the device terminals, at the input terminals of the circuitry

surrounding the device, or at the terminals of protective elements ahead of the device terminals or circuitry. Ideally, devices (which in certain designs can be semiconductor devices themselves) are intended to suppress EMP transients to levels below that which will cause damage to the sensitive devices. However, in practice, amplitude limiters have a limited response time and as a consequence there is a possibility of some "spill-over" or "leakage" through these devices before they clamp. Thus, in conducting tests where the EMP transient is applied ahead of the limiter there can be portions of the pulse applied directly to the sensitive device before limiting action of the protective device takes place.

Other phases of the system life cycle where EMP testing may be required include final hardness assurance prior to system delivery/operation, and maintenance testing to assure hardness during the operating life of the system.

While such tests apparently do not lead to immediate failures, there is reason to suspect that where transistors have been exposed to short impulses, such as static discharges, without immediate effects, the long-term reliability was seriously degraded.[1] Thus, the initially non-impairing EMP tests on critical components, either loose part or within equipments, over the life cycle might seriously reduce the operational readiness of critical defense systems, as well as introduce unanticipated maintenance costs. Such reduced reliability could be a factor in the possible loss of expensive prototype equipment, such as aircraft, which may be exposed to high-level EMP fields during acceptance tests.

Thus, a major problem is indicated by two apparently conflicting requirements, EMP hardness and long-term reliability. If the equipment is not EMP tested, it could fail during a nuclear threat; if it is EMP tested, it might fail because the life-time of sensitive components is radically shortened. The objective of the present program is to clarify the above problem

by determining whether stressing a semiconductor with EMP simulating pulses below the threshold of observable damage causes a degradation of reliability. Such degraded reliability is evidenced by a shorter lifetime (mean time to failure) for the stressed devices than for otherwise identical non-stressed ones.

2.2 Accelerated Life Testing - The Arrhenius Model

The above hypothesis may be tested in a straightforward manner. A sample of semiconductors which have been stressed at some fraction of the prompt damage threshold and a sample of identical but unstressed devices are run under the same operating conditions for a prolonged period of time. If a statistically significant number of stressed devices fail earlier than those which are unstressed the hypothesis is proven. However, since the normal failure rate for modern semiconductors may be one device per 10^7 hours or longer it will be necessary to run the test for times of this order unless the stressed devices fail very early or an impossibly large number of devices are tested. Fortunately, the necessary number of device operating hours may be obtained in attainable time spans by using a sufficiently large sample and accelerating the normal aging process. This technique of compressing test time is known as accelerated life testing.

The technique of accelerated life testing and its value in determining device reliability is well documented.[2-6] In this method, the failure mechanism of interest is identified and a stress is determined which will enhance this failure mechanism and cause it to proceed at a more rapid rate. For example, operating a semiconductor at an elevated ambient temperature while conducting heavy forward current will enhance the rate of migration of aluminum metallization and cause failures due to this mechanism to occur earlier than normally observed. In general, most of the failure mechanisms observed in semiconductor devices are accelerated by application of

thermal stress. The degree to which thermal stress accelerates device degradation may be expressed mathematically by the Arrhenius equation.

In a thermally activated process, the time rate of change of the process depends upon the temperature at which the process is taking place according to the Arrhenius equation[2]

$$R(T) = R_o e^{-\frac{E_A}{kT}} \qquad (1)$$

where

$R(T)$ = reaction rate

R_o = constant

E_A = activation energy (eV)

k = Boltzmann's constant (8.63×10^{-5} eV/^oK)

T = absolute temperature (^oK).

For the case of semiconductor device degradation it may be assumed that the process being thermally activated is evidenced by the degradation of some observable parameter. Thus, R may be interpreted as the rate of degradation of that parameter if E_A, the process activation energy is replaced by E_A', the related parameter degradation activation energy. Referring to Equation (1), it is evident that if the logarithm of R(T) is plotted against the reciprocal of the temperature (i.e., 1/T), the constants R_o and E_A/K represent the intercept and slope respectively of the resulting straight line.

Consider a semiconductor device tested at some high thermal stress at temperature T' until the parameter of interest has degraded by Q at time t'

$$Q = R(T')t' = R_o t' e^{-\frac{E_A}{kT'}} \qquad (2)$$

If the same device were tested to the same level of degradation at a lower, more normal temperature T, the test would require time t. For this condition

$$Q = R(T)t = R_o t\, e^{-\frac{E_A}{kT}} \tag{3}$$

Combining Equations (2) and (3) yields the time acceleration factor τ

$$\tau = t/t' = e^{-\frac{E_A}{k}\left(\frac{1}{T'} - \frac{1}{T}\right)} \tag{4}$$

Thus if a reliability test is conducted at temperature T' for t' hours, it is equivalent to t hours operating at the lower temperature T. Thus, $t = \tau t'$, which says that a test of reliability requiring 10^6 device hours at a low temperature, T, can be performed with the same results by running the test at an elevated temperature T' for only $10^6/\tau$ device hours.

In practice, acceleration factors greater than 10 are typical for temperature accelerated life testing of semiconductors. However, the upper bound obtainable is limited by many factors, the main one being that as the temperature level is increased, the mode of failure may change; that is, the part may fail for a different cause at the higher stress level. This leads to uncertainty in the prediction of how long the device would perform successfully under a normal stress level based on its observed performance under the high stress level.

There are two widely used accelerated life test procedures:

(1) Step-stress testing;
(2) Constant stress testing.

The step-stress test is conducted with a single sample group tested for fixed time intervals at successively higher stress levels until a sufficient number of devices have failed. Acceptance of the step-stress philosophy depends upon the assumption

that the degradation occurring at a given stress level is independent of prior levels. A variation of the common step-stress procedure is parallel step-stressing wherein the total sample group is divided into subsamples with each subsample being subjected to only a single stress level. This approach minimizes any influences of prior stress levels, if any, on the results obtained at a given stress level.

The step-stress procedure allows the determination of the time accelerating factor, τ, so that the test results at elevated temperature may be related back to the normal operating temperature. From the test results plots are made of the degradation of the observed parameter as a function of time for each of the thermal stress levels. Transformations are made if necessary to obtain straight lines whose slopes yield the rate of degradation at each temperature.[6] Using this information, the Arrhenius plot is made by plotting the logarithm of the rate of degradation vs. the reciprocal of absolute temperature. If the Arrhenius plot is a straight line, then a true acceleration exists. The activation energy is directly obtained from the slope of this line and Equation (4) yields the time acceleration factor. If a broken line results from the plotting procedure, then two or more distinct aging processes are present.

In constant stress testing a sample is placed on life test at a single stress level which is held constant for the full duration of the test. Measurements of key parameters are taken periodically to assess degradation. Depending on the test purpose, the experiment may consist of several test groups, each at a unique stress level. This latter procedure allows determination of acceleration factors and estimation of use condition failure rates.

2.3 EMP Damage Mechanisms and the Effect of Thermal Stress

The accelerated life test procedure described by the Arrhenius equation is valid for life degrading processes which are dependent upon thermal stress. The type of damage caused

in semiconductor devices by EMP pulse testing is of thermal origin[7] and as a result will almost certainly be influenced and enhanced by further thermal stress.

Many experimental studies[7-11] have shown that there is a threshold EMP power/energy level which will cause catastrophic or instant failure in a given semiconductor device. In these studies, empirical relationships, supported by theoretical considerations, have been derived from experimental data for the device burn-out or damage energy/power as a function of pulse width. It has been found experimentally (and verified theoretically) that the energy or power necessary for component damage varies as a function of the applied pulse width as illustrated in Figure 1 for a typical semiconductor device.

Other studies have been performed that show that the threshold power level necessary to cause junction failure in semiconductors is lower for multiple pulse exposure than that for a single pulse. This is shown in Figure 2 which shows the pulse power necessary to induce failure in a 2N2222 type transistor using single, double and triple pulses. In the analysis carried out to obtain these curves, the interval between pulses was assumed sufficiently short to prevent junction cooling. Thus, the junction heating produced by the multiple pulsing was cumulative and perhaps explains the reason why the difference between single-pulse and triple-pulse failure thresholds is less than the statistical spread in data points for a single-pulse failure.

In other experiments,[11] the cumulative effects of repeated EMP pulse testing was studied in which the sequence of pulses applied were spaced far enough apart to preclude cumulative heating effects at the device junction. Figure 3 shows the results of this repeated pulse testing <u>after</u> initiating component damage (defined here as a specified drop in gain) by the <u>first</u> pulse in the sequence. The two curves in the figure show the further degradation in gain caused by the following

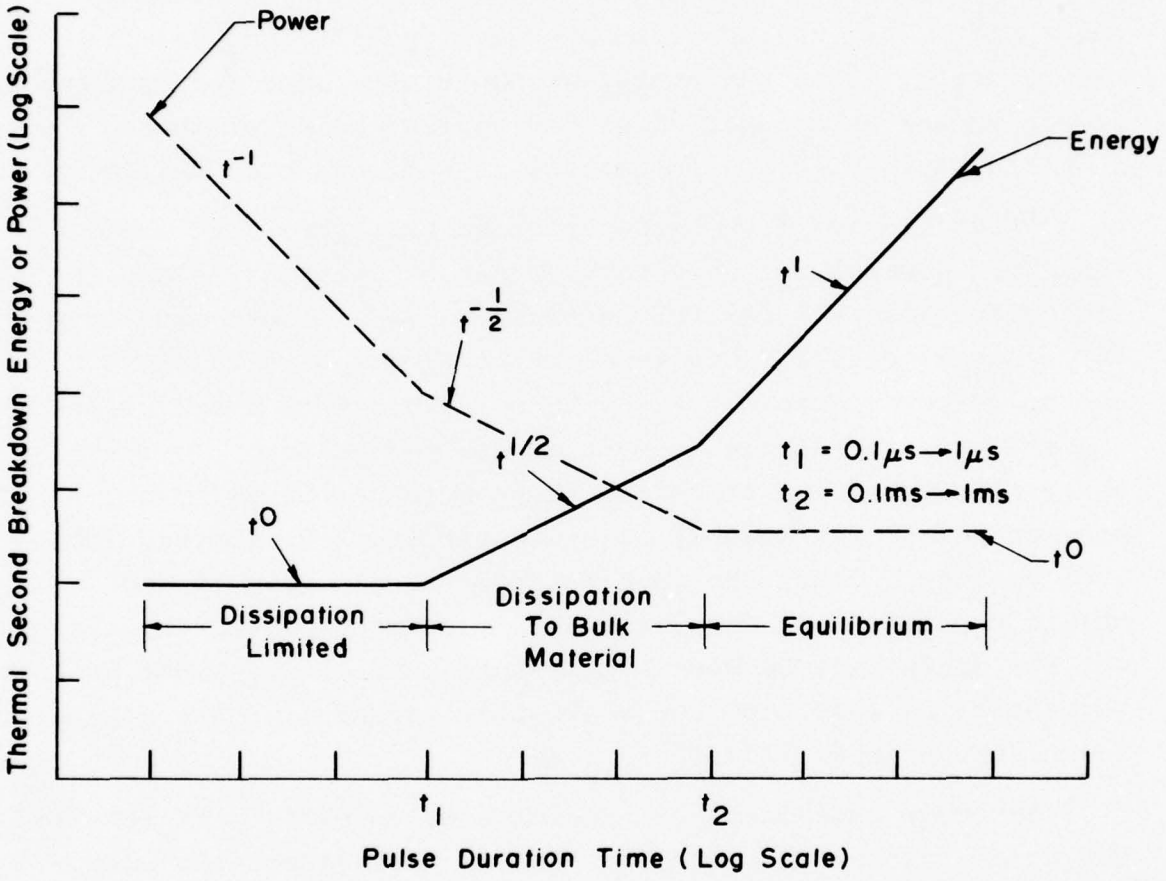

Fig.1 TYPICAL FAILURE LEVEL RELATIONSHIPS FOR THERMAL SECOND BREAKDOWN IN SEMICONDUCTOR JUNCTIONS

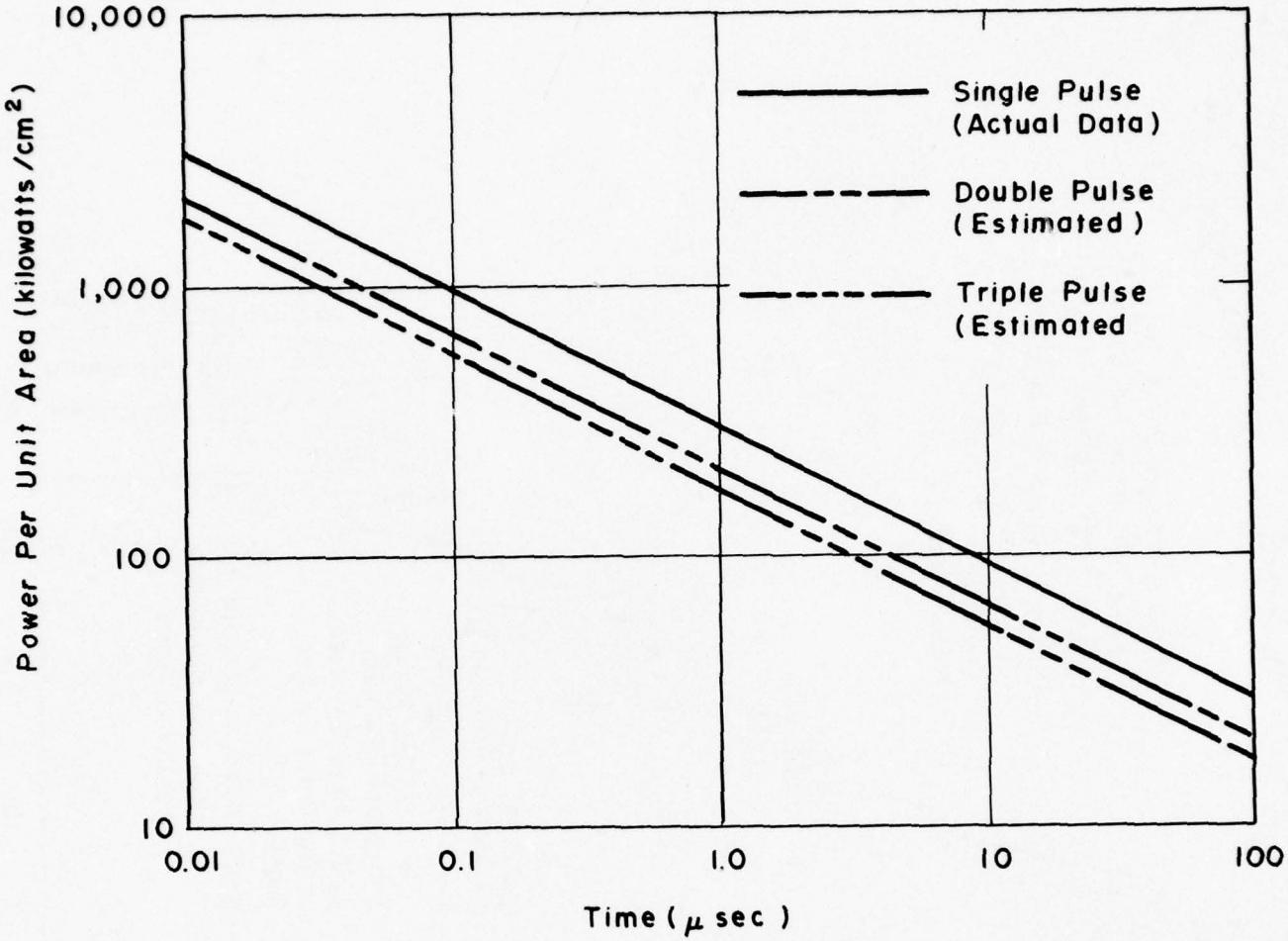

Fig. 2 MULTIPLE EMP PULSE DAMAGE THRESHOLDS FOR TRANSISTORS

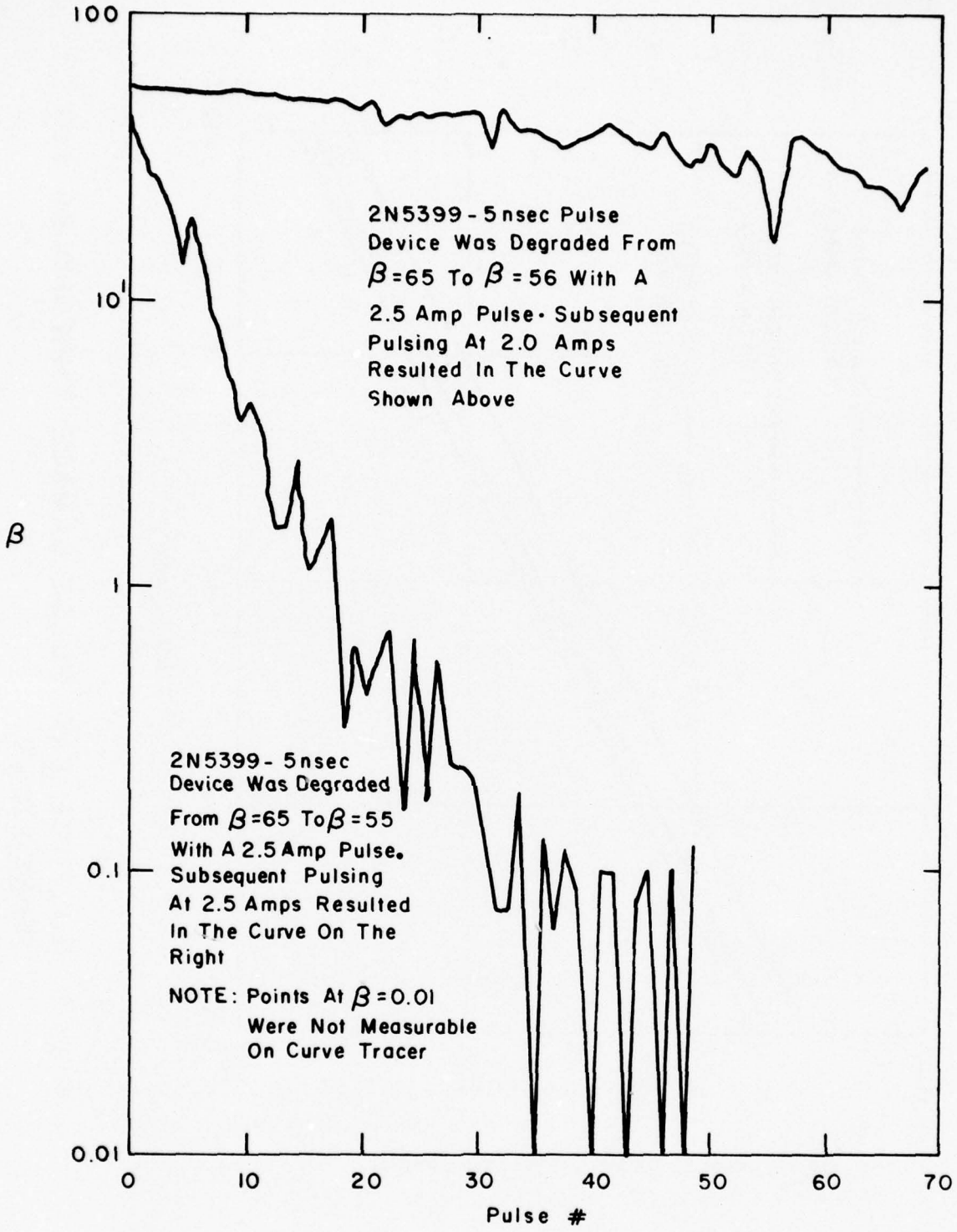

Fig. 3 GAIN DEGRADATION FROM CURRENT PULSES FOR TWO CONDITIONS

pulses for each of two different conditions. For the lower curve, all pulses following the first pulse were also at the damage threshold level. The upper curve was obtained by pulsing the device with pulse power 0.8 times the threshold level after the first damage level pulse. Comparison of the two curves shows that reducing the amplitude of pulses applied after damage initiation merely reduces the rate at which additional damage or parameter degradation occurs.

All of these experimentally observed results are consistent with the model that EMP induced damage in a semiconductor is thermal damage resulting from the dissipation of an excessive amount of energy in a short time. The large amount of energy in an EMP pulse when deposited within the semiconductor may cause micro-plasma formation, local hot spots, and even melting of the silicon. In the most extreme case, a melt channel may form through the junction causing the junction to be short circuited and the device to fail catastrophically. In a less extreme case, localized heating may cause the formation of a microscopic high resistance channel through the junction or over its surface. Such a channel would result in increased leakage and degraded h_{FE} in a transistor but not in complete failure. It is clear that the EMP stress level for which a device will be damaged depends upon its geometry and construction details. Devices with larger junction areas will, in general, tolerate higher EMP energy levels than devices with smaller junctions since the power is dissipated over a larger area resulting in a smaller temperature rise. Some variation in the EMP damage threshold for a given device type is to be expected due to small unavoidable variations in their structure. Any structural or material nonuniformity will result in field nonuniformity and hence, preferential current channeling. Variation in the current distribution effects the power dissipation and hence the EMP damage threshold. Hence, it is expected that the EMP damage threshold for a device type will

have some statistical distribution. Since there are multiple, inter-related factors which may influence the damage threshold a log normal distribution might reasonably be expected.[2]

To evaluate the effects of EMP stressing on reliability via an accelerated life test, it is necessary that the damage or degradation caused by the EMP be enhanced by application of thermal stress. As discussed above, the EMP stress causes formation of some nonuniformity in the semiconductor material by overheating it. This may vary from complete melting and failure to partial melting or modification of the semiconductor material in a small localized area. Biasing the device to carry current at an elevated stressing temperature will worsen such defects. The elevated temperature decreases the resistance of any channels or weak spots created by the EMP stressing thus causing increased current flow at the site of the defect with attendant further degradation. Moreover, the thermal conductivity of silicon is a strong function of temperature varying from 1.56 watts/cm-^{o}K at 300°K to 0.310 watts/cm-^{o}K at 1000°K.[7] Increased current through EMP induced micro-channels or weak spots will cause increased heating at these locations. At an elevated test temperature the lowered thermal conductivity will cause a relatively higher local temperature at the defect sites than would occur for the higher thermal conductivity at normal operating temperatures. Again, this increased local heating increases the rate of degradation at the point of EMP damage. Still another way in which thermal stress may accelerate EMP induced damage is through the mechanism of diffusion enhancement. In gold doped semiconductor devices there is a strong possibility that one of the degradation modes caused by EMP is increased leakage due to the movement of gold atoms from lattice sites to interstitial positions.[12] Thermal stress will cause the further diffusion of these gold atoms in the material resulting in increased leakage. Since the EMP induced damage modes are subject to thermal enhancement, it is valid to look

at the long term degradation and failure caused by EMP with the time compression technique of accelerated life testing.

2.4 Semiconductor Life Models

In determining the effect of EMP stressing on device life it is necessary to adopt a model to be used in analyzing and interpreting the data obtained from accelerated life tests. Such a model for device life consists of a life expectancy distribution or failure density function for the device and relationships between the parameters of this distribution and the accelerating variables or stressing agents. One model which results from observation of the life of a device under normal operating conditions is the exponential model.

Observation of the life cycle of most devices indicates that there are three periods in time characterized by different failure rate behavior. During the very early life there is a larger than normal failure rate which decreases with time due to the failure of those devices which are commonly termed "freaks." The semiconductor industry uses the term freaks to describe devices which are extremely weak due to manufacturing flaws or other quality defects and are normally removed from the device population by burn-in procedures and screens. The midlife period is characterized by a long period of time during which the failure rate is nearly constant as chance failures due to minor hidden weaknesses or defects are observed. For semiconductors the failure rate during this interval is very low approaching values of 10^{-5} to 10^{-7} device failures per hour. Finally, a period of increasing failure rate is expected as devices begin to wear out and fail. This life history is illustrated in Figure 4 and may be used in deriving the exponential distribution function.

It is noted that the midlife period failure rate is essentially a constant given by λ. This says that at any instant in time there is a constant "force of failure" given by

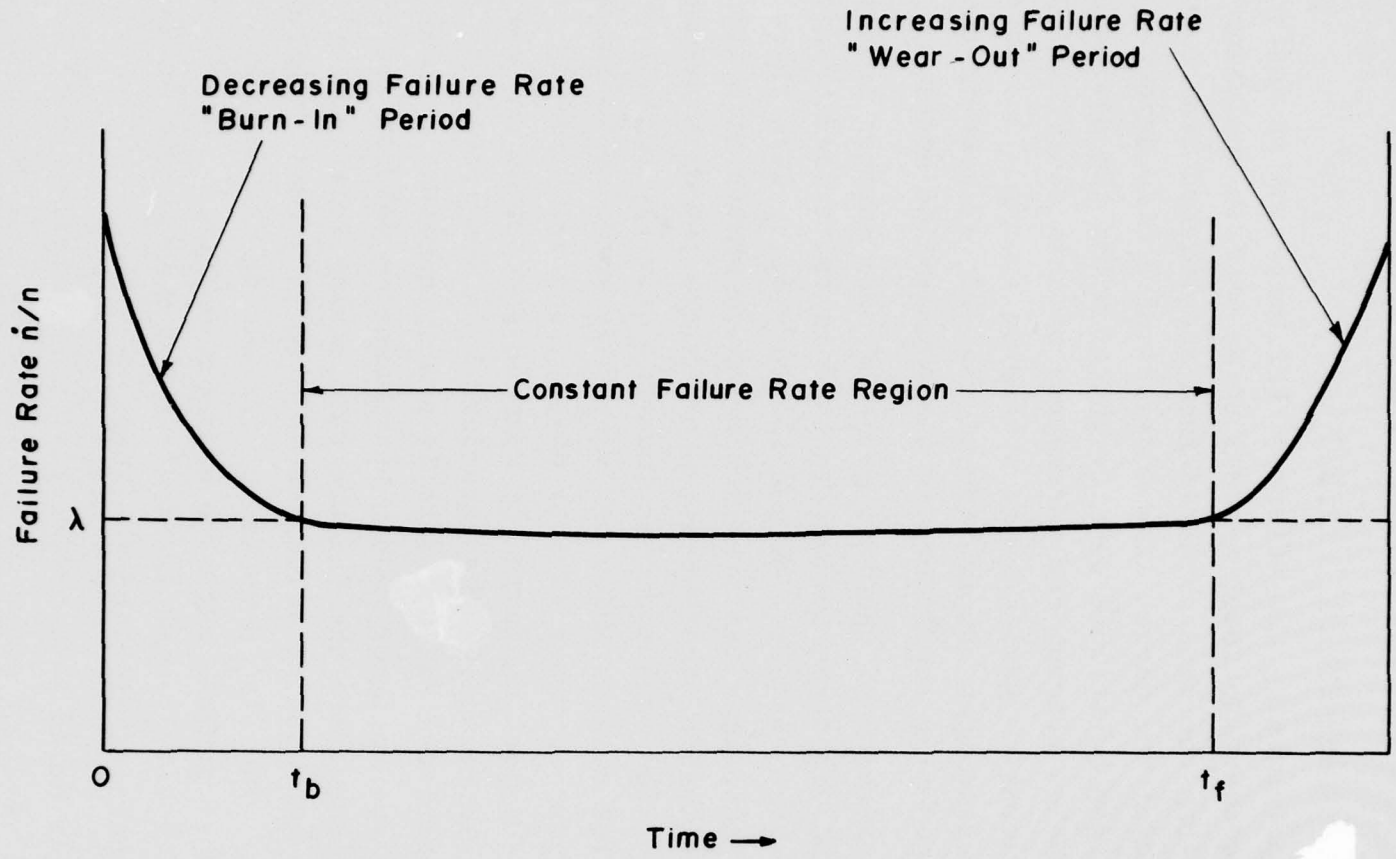

Fig. 4 FAILURE TYPE AS A FUNCTION OF TIME

$$\dot{n} = -\lambda n \tag{5}$$

acting throughout the time period considered. Integrating Equation (1) produces the result that at any instant of time, t, ($t \geq t_b$; where t_b is defined in Figure 1) the number of devices, n, that survive a period of time, t, is given by:

$$n(t) = N_b e^{-\lambda(t-t_b)} \quad t \geq t_b \tag{6}$$

where

N_b = number of devices at $t \approx t_b$.

By dividing n by N_b in Equation (6) we obtain the ratio of surviving devices, n, relative to the number of initial sample devices, N_b, at time, t_b. Reliability engineers define this as the exponential probability distribution function $P_s(t,\lambda)$ given by:

$$P_s(t,\lambda) = \frac{n}{N_b} = e^{-\lambda t} \tag{7}$$

Reliability of devices is measured in terms of this distribution function in which $1/\lambda$ is the expected time to failure or MTTF (*mean time to failure*). Alternatively, this function may be viewed as the probability that n devices of a given sample lot, N_b, will survive after a period of time, t. It is to be noted here that Equation (7) is applicable only if early "wear-in" failures (the "freak" population occuring over the period 0 to t_b as shown in Figure 4) have been screened out. Thus in any reliability study and/or analysis carried out using this probability model, all test sample lots must be screened or "burned-in" prior to conducting the proposed reliability testing.

Another model of semiconductor life is the lognormal model. The lognormal failure density function occurs repeatedly in thermally accelereated life tests of semiconductor components and is characterized by a failure rate which declines with time.

For the lognormal life distribution the population fraction F(t) failing as a function of age is described by the dumulative distribution function[4]

$$F(t) = \Phi\left[\frac{\log_{10}(t) - \mu}{\sigma}\right] \tag{8}$$

where Φ is the standard normal cumulative distribution function. The parameter, μ, the logarithmic mean, is the mean of the logarithms of the lifetimes of the individual members of the population. The parameter, σ, the logarithmic standard deviation, is the standard deviation of the logarithms of the times to failure of the population members. It may be noted that the median of the lognormal distribution is related to the logarithmic mean by the relation

$$t_{0.50} = \text{antilog } \mu. \tag{9}$$

The probability density function of the lognormal distribution is obtained by differentiating (8) to give

$$f(t) = \frac{0.4343}{\sigma t}\ \phi\left[\frac{\log_{10}(t) - \mu}{\sigma}\right] \tag{10}$$

where

$$\phi(Z) = \frac{1}{\sqrt{2\pi}}\ e^{-Z^2/2} \tag{11}$$

is the probability density function of the standard normal distribution. The mean of this distribution, often useful when seeking the average life for the population (mean time to failure) is given by[4]

$$\bar{t} = \int_0^\infty tf(t)dt = \text{antilog } (\mu + 1.151\sigma^2). \tag{12}$$

It will be seen in Sections 4.1 and 4.2 that the results of this program indicate lognormal life distributions for the semiconductors studied.

3.0 THE EXPERIMENTAL PROGRAM

3.1 Introduction

A comprehensive experimental program based upon the accelerated life test concept was designed and carried out to determine the effect of EMP stressing upon the reliability (life expectancy) of selected semiconductor devices. The experiment was divided into two major phases as outlined below.

Phase I: Preliminary Device Selection and Evaluation

- Select five devices for evaluation and testing;
- Determine device damage constants;
- EMP stress selected devices;
- Step stress test five selected device types after EMP stressing;
- Select two device types for long term life test based upon their behavior during the step stress test.

Phase II: Long Term Constant Stress Accelerated Life Test

- Determine EMP damage constant for devices to be tested;
- EMP stress device samples;
- Accelerated life test stressed and unstressed devices;
- Analyze data.

3.2 Phase I - Preliminary Device Selection and Evaluation

Data on numerous bipolar transistors and diodes was carefully examined to choose five device types for preliminary evaluation. Devices which were considered are listed in Tables 1 and 2. The five device types chosen for preliminary testing were the 2N916, 2N918, and the 2N2222 bipolar transistors and the 1N914 and 1N4148 diodes. The selection of these particular devices was based upon their 1) wide use, 2) available reliability data, 3) well defined EMP damage threshold, and 4) damage

TABLE 1 CANDIDATE DIODES

Type Designation	COMMENTS		
	General	EMP Damage Threshold[13]	Reliability[14]
IN456	Small Signal Diode	Well behaved damage data. Doesn't follow $t^{-\frac{1}{2}}$ curve.	No data on record.
IN482	Small Signal Diode	Well behaved damage data. Doesn't follow $t^{-\frac{1}{2}}$ curve.	No data on record.
IN486	Small Signal Diode	Good damage data.	No failures in 3.2×10^{7} cumulative device hours
IN660		Very well behaved damage data. Considered great.	No data on record.
IN914		Very well behaved damage data.	One failure in 3.7×10^{6} cumulative device hours
IN964B	Diffused Zener 13 v breakdown.	Good damage data with consistent damage threshold.	No failures in 1.5×10^{5} cumulative device hours
IN965B		Well behaved damage data around 1.0 μsec.	No failures in 1.4×10^{5} cumulative device hours
IN970	23 v breakdown.	Well behaved damage data.	No failures in 9.1×10^{4} cumulative device hours
IN972	28 v breakdown.	Well behaved damage data.	No failures in 7.7×10^{4} cumulative device hours
IN973		Not well behaved. Erratic damage data.	No failures in 4.7×10^{4} cumulative device hours
IN974		Well behaved damage data. Doesn't follow $t^{-\frac{1}{2}}$ curve.	No failures in 4×10^{3} cumulative device hours

TABLE 1 CANDIDATE DIODES (Cont.)

Type Designation	COMMENTS		
	General	EMP Damage Threshold[13]	Reliability[14]
IN3064	Switching diode. Gold doped.	Well behaved damage data.	No failures in 4.4×10^5 cumulative device hours
IN3600	Gold doped.	Well behaved damage data.	No failures in 8.7×10^6 cumulative device hours
IN4148		Quite a bit of scatter in damage data. May not be typical of behavior though. GE has done alot of testing with good results.	Four (4) failures in 1.86×10^8 cumulative device hours.
IN4152		Well behaved damage data.	No data on record.
IN4154		Good damage data.	No data on record.
IN4244		Damage data not good.	No data on record.
IN4450		Good damage data.	No data on record.
IN4727		Good damage data.	No data on record.

TABLE 2 CANDIDATE TRANSISTORS

Type Designation	COMMENTS		
	General	EMP Damage Threshold[13]	Reliability[14]
2N697	BV_{CB} = 60 v	Well behaved damage data. High data point at 10 μsec.	No data on record.
2N834A	Gold doped. BV_{CE} = 40 v	Very well behaved damage data. Follows $t^{-\frac{1}{2}}$ curve closely.	No data on record.
2N869A	Not gold doped.	Well behaved damage data.	No data on record.
2N916	Not gold doped. BV_{CE} = 45 v.	Good damage data.	One failure in 3.5×10^6 cumulative device hours
2N918	Gold doped.	Good damage data.	No failures in 8.2×10^6 cumulative device hours
2N930	Low noise. Not gold doped. BV_{CE} = 45 v	Very well behaved damage data.	No failures in 1.9×10^5 cumulative device hours
2N2222	Not gold doped.	Well behaved damage data. Many years of EMP testing.	No failures in 2.3×10^7 cumulative device hours for 2N2222. Ten (10) failures in 7.9×10^6 cumulative device hours for JTX 2N2222A.
2N2481		Damage data scattered and erratic.	No data on record.
2N2484		Damage data scattered and erratic.	No failures in 7.4×10^5 cumulative device hours

TABLE 2 CANDIDATE TRANSISTORS (Cont.)

Type Designation	COMMENTS		
	General	EMP Damage Threshold[13]	Reliability[14]
2N2905	Interdigitated. High device. Not gold doped. BV_{CB} = 60 v.	Damage data good.	Four (4) failures in 5.3×10^6 cumulative device hours.
2N2907	Same as above; different can.	Damage data good.	No failures in 1.1×10^7 cumulative device hours for 2N2907. Four (4) failures in 3.7×10^6 cumulative device hours for JTX 2N2907A.
2N3019	Not gold doped. BV_{CB} = 140 v.	Good damage data.	One (1) failure in 2.3×10^5 cumulative device hours for JTX 2N3019A.
2N3114		Lot of scatter in damage data.	No data on record.
2N346B	Not gold doped.	Damage data good.	No data on record.
2N3700		Damage data erratic.	No failures in 2.8×10^4 cumulative device hours for JTX 2N3700.

threshold power level being within the range of available pulse generation equipment. The latter requirement is dictated by the need to pulse a number of the candidate devices to the point of observed damage to assure adherence of the sample to the published damage specifications. Electrical specifications for these devices and their EMP damage data are given in Tables 3 and 4, respectively.

Five each of the candidate devices purchased for preliminary life testing (JTX 1N914, JTX 1N4148, JTX 2N918, JAN 2N916, and JTX 2N2222A) were tested to destruction to determine their respective damage constants by applying reverse biasing pulses of 1 μsec duration. The pulses were generated by a Hewlett Packard laboratory pulse generator and amplified to the required level by an Amplifier Research Model 1000L broadband RF amplifier. Voltage across the device and current through it were carefully monitored using storage oscilloscopes and the point of irreversible damage was noted for each device. For the transistors this was taken as the reverse biasing pulse power (1 μsec pulse width) applied across the emitter-base junction which caused h_{FE} to decrease by at least 10 percent. In addition, it was required that further pulsing at this power level caused h_{FE} to irreversibly decrease with each successive pulse. For diodes, the damage point was taken as the reverse biasing pulse power (1 μsec pulse width) required to cause an observed increase in the reverse leakage current. This increase was always by a factor of at least 2 at one or both of the measurement points (20 and 80 volts reverse bias). The observation of increased leakage was always accompanied by a decrease in the reverse breakdown voltage and in all cases additional pulses at this level resulted in diode burnout. The average damage power levels determined by these criteria are given in Table 5.

One half of each of the remaining groups of devices were stressed by subjecting them to five (5) 1 μsec pulses at one-half the average damage power noted in Table 5.

TABLE 3 DEVICE SPECIFICATIONS

DIODES (Data at 25°C)

TYPE	V_F@10ma	V_{BR}@100µa	PD	I_{Fmax}	I_R@20V@150°C
1N914	1 V	>100 V	250 mW Derate 1.4 mW/C°	75 ma	<50 µa
1N4148	1V	>100V	500 mW Derate 2.85 mW/C°	75 ma	<50 µa

TRANSISTORS

TYPE	$V_{(BV)}$CBO	$V_{(BR)}$EBO I_C=10µa	$V_{(BR)}$CEO	h_{FE} V_{CE} = 1.0	P_D@25°C
2N916	45 Vmin I_C = 10 µa	5 Vmin	25 Vmin I_C = 25 ma	50min-200max I_C = 10 ma	360 mW Derate 2.06 mW/C°
2N918	30 Vmin I_C = 1 µa	3 Vmin	15 Vmin I_C = 3 ma	20 Vmin I_C = 3 ma	200 mV Derate 1.14 mW/C°
2N2222A	60 Vmin I_C = 10 µa	5 Vmin	30 Vmin I_C = 10 µa	50 min I_C = 150 ma	500 mW Derate 3.33 mW/C°

TABLE 4

EMP DAMAGE CONSTANTS FOR CANDIDATE DEVICES

Device	Wunsch Constant EB Reverse, AC Reverse	Damage Constant (Curve Fit τ = 1μs)	Breakdown Voltage (τ = 1μs)
1N914	96	54.8	127 volts
1N4148	19.4	16.9	106.6
2N916	51	51.1	23
2N918	8.6	6.24	16.8
2N2222	82	91	~ 23 *

* Interpolated

TABLE 5

EMP TEST RESULTS

Device	Average Failure Power (1 μsec)	Standard Deviation	Published Damage Constant
1N914 JTX	83.75 Watts	11.0	54.8
1N4148 JTX	155.5	11.6	16.9
2N916 JAN	26.1	2.61	51.1
2N918 JTX	4.52	0.15	6.24
2N2222A JTX	68.22	1.91	91.0

The above stressed devices, along with a similar number of unstressed control devices, were placed in a temperature controlled oven on specially constructed heat resistant test circuit boards using heat resistant sockets. The biasing circuits and control circuitry to allow switching from bias to parameter measurement are fully described in Appendix A. The devices under test were forward biased so that internal dissipation raised the junction to 100°C and oven temperature was maintained according to the following thermal step stress schedule:

Day	Oven Temperature	Junction temperature
1	150°C	250°C
2	162°C	262°C
3	175°C	275°C
4	189°C	289°C
5	203°C	303°C
6	218°C	318°C

After completion of the above schedule, the devices were maintained for an additional ten (1) days at 318°C junction temperature. At the end of the sixteen (16) day period (384 hours) the JTX 2N2222A's were removed from the test since the leakage current became too high to allow monitoring h_{FE}.

Bias current to the JAN 2N916's and JTX 2N918's was increased to obtain a 343°C junction temperature and testing was continued for an additional 204 hours with the JTX 2N918 and JAN 2N916 junctions at 343°C and the diode junctions at 318°C. This increase in junction temperature was made in an attempt to obtain more failures in the limited time allotted to this task. The following summarizes the test conditions.

Device Tested	Number Stressed	Number Unstressed	Total Device Hours	Device Hours Above 300°C
JTX 2N914	8	8	9,408	7,872
JTX 1N4148	11	13	14,112	11,808
JTX 2N918	10	10	11,760	9,840
JAN 2N916	5	5	5,880	4,920
JTX 2N2222A	8	8	6,144	4,608

At the conclusion of the step stress testing there was only one confirmed failure among the transistors, an unstressed JTX 2N918 which failed due to infant mortality during curve tracer measurements before any thermal stress was applied. Several other transistors, both stressed and unstressed, appeared to fail (degraded h_{FE}), while at an oven temperature of 218°C. However, upon testing these devices at room temperature no performance degradation was observed. It was determined that the observed degradation at oven temperatures above 189°C resulted from the poor electrical contact caused by the softening of the solder used to connect the transistor test sockets to the printed circuit board. There was, however, no evidence of failure in the device under test. Similar behavior was observed in a small group of JTX 1N4148 diodes with false indications of failure above 189°C oven temperature.

The JTX 1N914 diodes showed the only true failures under thermal stressing. Five stressed devices and one unstressed device failed at the end of 24 hours of heating at a junction

temperature of 275°C (oven temperature = 175°C). The mode of failure was the appearance of very high forward resistance. However, if the forward voltage was increased momentarily to 20 volts or more, normal diode behavior was restored. From this very limited data, it would appear that the pulse stressing did have a degrading effect on device reliability.

The preliminary screening test indicated that, of the transistors, the 2N918 was the best choice for the final test since it had the narrowest range of damage constant and was well behaved in the test apparatus at elevated temperatures. The 2N2222A exhibited a very large leakage current at elevated temperature making measurement of h_{FE} difficult and inaccurate. Moreover, this device has a very high probability of oscillation in the test apparatus, particularly at high temperature where h_{FE} rises. The 2N916 was well behaved at high temperature but had a larger spread in damage constant than the 2N918 thus making it difficult to stress at 0.9 of the damage level without losing an excessive number of devices. The screening test suggested the use of the 1N914 diode in the final life test since it appeared to show pulse stress related degradation while the 1N4148 gave no such clear indication.

It had been hoped that the preliminary step stress test would yield an estimate of the time acceleration factor by allowing construction of an Arrhenius plot to obtain the activation energy for use in Equation (4). However, construction of an Arrhenius plot requires a large sample size tested for sufficient time at each temperature to yield a distribution of failures with temperature. Our preliminary screening tests were unable to give a sufficient number of failures due to the very small sample size (approximately 10 of each device type) and limited operating time necessitated by available funds. However, it was not considered essential to know the acceleration factor in view of the fact that the objective in the final test was to determine whether EMP stressing effects operating

lifetime (reliability) on a comparative rather than an absolute basis. It was for this reason that a control group of unstressed devices were operated at the same time and under the exact same operating conditions as the stressed group during the final test. For observed differences in relative reliability, a numerical estimate of the degradation of mean time to failure can be made using the measured stressing temperature, running time, estimated activation energy, and the Arrhenius model to calculate the approximate accelerating factor.

Finally, the preliminary test also served the useful function of checking the test equipment to be used in the long term life test. The only serious deficiency uncovered was the weakness of the solder alloy used at elevated temperature. This critical defect was corrected by replacing all solder with a silver-bearing eutectic which has been shown to be completely reliable for the temperature range of interest.

3.3 Phase II - Long Term, Constant Stress Accelerated Life Test

Four hundred (400) Texas Instruments JTX 1N914 diodes and 375 Texas Instruments JAN 2N918 transistors were obtained for the final life test. To insure best possible uniformity among the devices, all devices of a type were from the same date code/lot number. (It was not possible to obtain the JTX version of the 2N918 within the time frame of the experiment and as a result, available JAN devices were substituted.)

To determine the effects of EMP stressing on device reliability, a finite population of EMP stressed devices and unstressed control devices were placed on test to allow comparison of their life behavior. The total number of EMP stressed devices were divided into two equal groups. One group was stressed to within a large fraction of the damage threshold of the device. The second group was stressed at a significantly smaller level. In this way, information was obtained on the effect of stressing level on the device

reliability. Limitations on available funds and the size of the test apparatus dictated that no more than 256 of each of the two device types be placed on test.

It is advantageous to have an identical number of device operating hours for each of the two stressed groups and for the control group. Equal group size simplifies comparison of failure rates between the groups in the absence of knowledge of the time accelerating factor. Moreover, any variation in failure rates between the stressed and unstressed groups is immediately evident since it is clearly observable without need to resort to statistical methods to relate occurrences observed in groups of different size. For the above reasons, 84 devices were life tested at each of the two stress levels while 84 unstressed but otherwise identical devices served as a control group during the final life test.

3.3.1 Device Considerations

The use of elevated temperature in thermally accelerated life testing requires a knowledge of the temperatures at which abnormal failures occur within the device due to such structural limitations as the melting of eutectic bonds. The preliminary stress test indicated that such failures do not appear at the temperatures used. Moreover, private discussions with Dr. Conrad H. Zierdt, Jr., who has gained considerable experience with accelerated life testing at Bell Laboratories, confirmed that a 300°C test temperature for glass encapsulated diodes and hermetically sealed metal can transistors is routine and should cause no problems.[15]

Further information was obtained from the manufacturer of the devices, Texas Instruments. The JAN 2N918 was described as a planar epitaxial high frequency transistor which is very shallowly diffused. The good high frequency behavior is obtained by gold doping. The emitter and base contacts are made with a closely spaced, interdigital aluminum metallization.

High temperature operation of the device may accelerate migration of the aluminum metallization. No information was available on the normal failure mechanism of the device since those failure modes which are readily observable are usually due to manufacturing defects rather than an inherent property of the device. True end of life failures are usually due to some unobservable obscure mechanism. It is possible that in some of these cases, aluminum penetrates the very shallow junction and causes failure. The manufacturer does not test the 2N918 above 200°C since testing beyond this is not required to meet military specifications. However, there should be no problem with device integrity even at 300°C. The gold eutectic which bonds the die to the header melts at 400°C and the aluminum silicon eutectic which is present melts near 500°C.[16] The device identification sheet for the 2N918 transistor listing the non-proprietary fabrication information is shown in Figure 5.

The JTX 1N914 is described as a planar, gold doped, high speed switching diode having as an anode a 4 mil circle diffusion 0.3 mil deep. The starting material is 3-5 ohm centimeter silicon. The epitaxial layer is 0.5 mil thick grown on 0.01 ohm centimeter substrate. There should be no problem testing this device at 300°C since the lowest melting point material present is a 380°C eutectic used in bonding the die to the dumet plug.[12]

Limited reliability information on the above devices was obtained from the quality assurance group at Texas Instruments.[17] The information obtained represents the results of lot acceptance tests performed by Texas Instruments. The JAN 2N918 shows a typical failure rate of 0.980 per 1000 hours based upon 102,000 device hours operating at 200 mW dissipation. Storage life tests at 200°C yielded a failure rate of 1.299 per 1000 hours based upon 154,000 device hours. Tests on the 1N4148 which is identical in construction to the 1N914 showed a failure rate of 0.211 per 1000 hours based on 474,500 device hours. Texas Instruments states that this data is applicable to the 1N914 as well.

Silicon Slice	Geometry
Type: Epitaxial, N on N+	Base Area ≈ 7 Sq. Mils Emitter Area ≈ 1 Sq. Mils
Oxide Thickness: 7000 Å ± 2000 Å	
Base Diffusion Dopant: Boron Depth: 10000 Å ± 5000 Å	
Emitter Diffusion Dopant: Phosphorous Depth: 7500 Å ± 5000 Å	
Top Metal 10,000 Å Type: Aluminum, ± 3000 Å	
Back Metal 2000 Å + 2000 Å - 1000 Å Type: Gold,	
Passivation Type: Nitride Thickness: 2000 Å + 1200 Å - 800 Å	
Die Size .010 x .015 in.	Device Type: 2N918

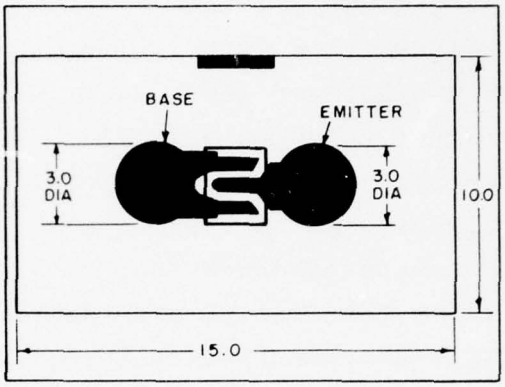

Fig. 5 2N918 GEOMETRY AND FABRICATION INFORMATION

3.3.2 Determination of Device EMP Damage Thresholds

In order to stress the devices for the final life test to the required fractions of the damage threshold it was necessary to determine the mean damage energy for the particular lots of semiconductors purchased. It is not sufficient to use the published damage data for the device type since the damage threshold varies widely from production lot to production lot and even among devices from the same lot.

The 2N918's have a low damage threshold and may be stressed to destruction with a laboratory pulse generator such as the Hewlett-Packard Model 214A. A simple test fixture was constructed to allow switching the transistor leads from the pulse generator output to the input of a transistor curve tracer. A negative going 1 μsec pulse was applied to the base with the emitter grounded and the collector floating, thus reverse biasing the emitter-base junction. After each pulse the transistor characteristics were monitored to detect any change in h_{FE}. If no degradation was evident the pulse energy was increased and the test repeated until degradation in h_{FE} was noted. As in the preliminary tests, damage was defined as a 10% or more reduction in h_{FE} with continued degradation for each additional pulse. The validity of the resulting damage threshold is dependent upon the assumption that the result observed at any given pulse level is independent of the pulses preceding it. For this reason, sufficient time was allowed between pulses to permit the transistor to return to ambient temperature thus minimizing any cumulative effect due to heating. A total of 61 JAN 2N918 transistors were tested to failure to obtain sufficient data to allow determination of the distribution of the damage threshold. The data obtained is tabulated in Appendix B. The mean damage energy is 7.01 μJoules with a standard deviation, σ, of 0.37 μJoules. This compares favorably with the published damage energy of 6.24 μJoules.

The damage constant data may be grouped into classes and the class frequency plotted to form the frequency histogram shown by the broken lines in Figure 6. From this histogram a frequency polygon is obtained by plotting a line graph of class frequency against class mark (midpoint of class interval). When the frequency polygon is smoothed a relative frequency distribution shown by the solid curve of Figure 6 results. This curve, representing the distribution of the threshold EMP damage energy in the 61 unit sample of JAN 2N918 transistors, appears to be approximately a normal distribution. The degree to which this approaches a normal distribution may be judged by plotting on a normal probability scale the cumulative relative frequency derived from Figure 6 against the damage energy. This has been done in Figure 7. The degree to which the plotted points conform to a straight line indicates the extent to which the distribution approaches a normal distribution. From Figure 7 it is clear that the data falls remarkably close to a straight line. Hence the distribution of damage constants is very nearly normal or Gaussian. A mathematical evaluation of the "goodness of fit" carried out in Appendix C using the chi-square test indicates the distribution is normal at the 95% confidence level.

Another distribution function which may be considered logical for the threshold damage energy is the lognormal distribution. For small values of logarithmic standard deviation, the normal and lognormal distributions are quite similar. The degree to which the data fits a lognormal distribution is seen by plotting cumulative relative frequency on a normal probability scale against the logarithm of the damage energy. As seen in Figure 8 the result deviates only slightly from a straight line indicating a relatively good fit to the lognormal distribution. From the straight line fit, the logarithmic mean μ and the logarithmic standard deviation may be determined as 0.844 and 0.023 μJoules, respectively. The logarithmic standard deviation is small as expected.

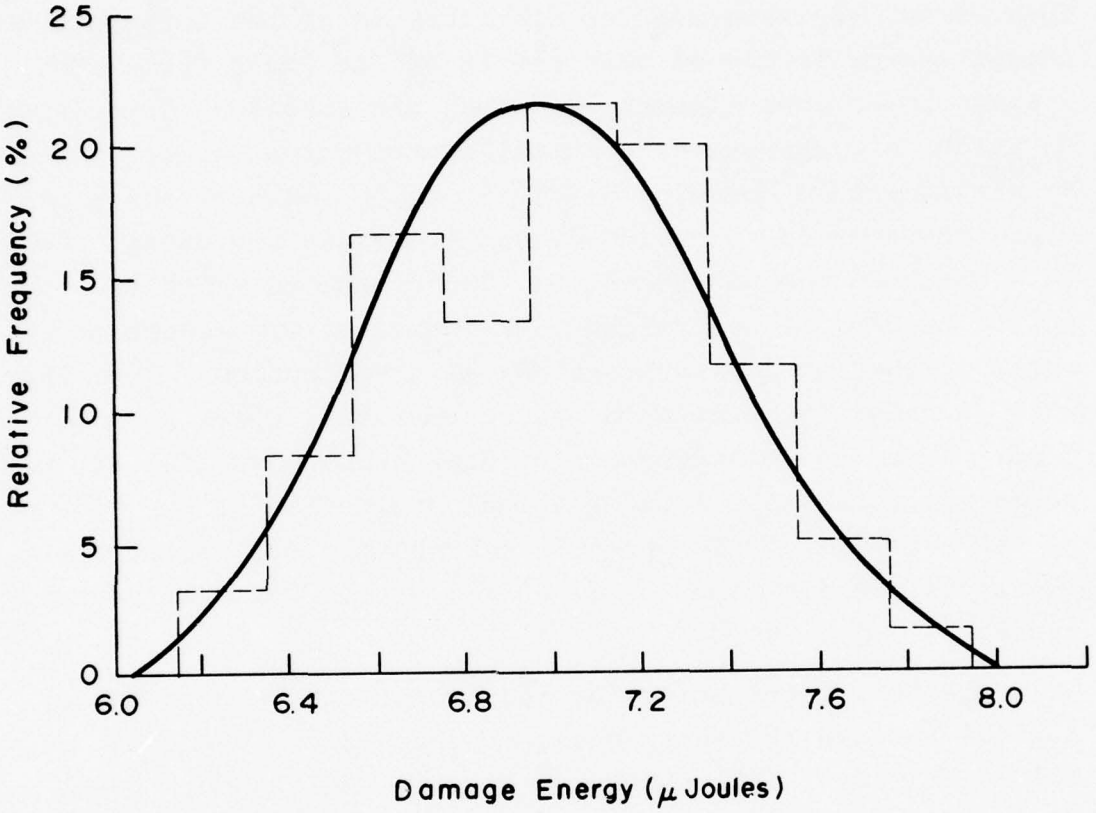

Fig. 6 JAN 2N918 DAMAGE ENERGY DISTRIBUTION

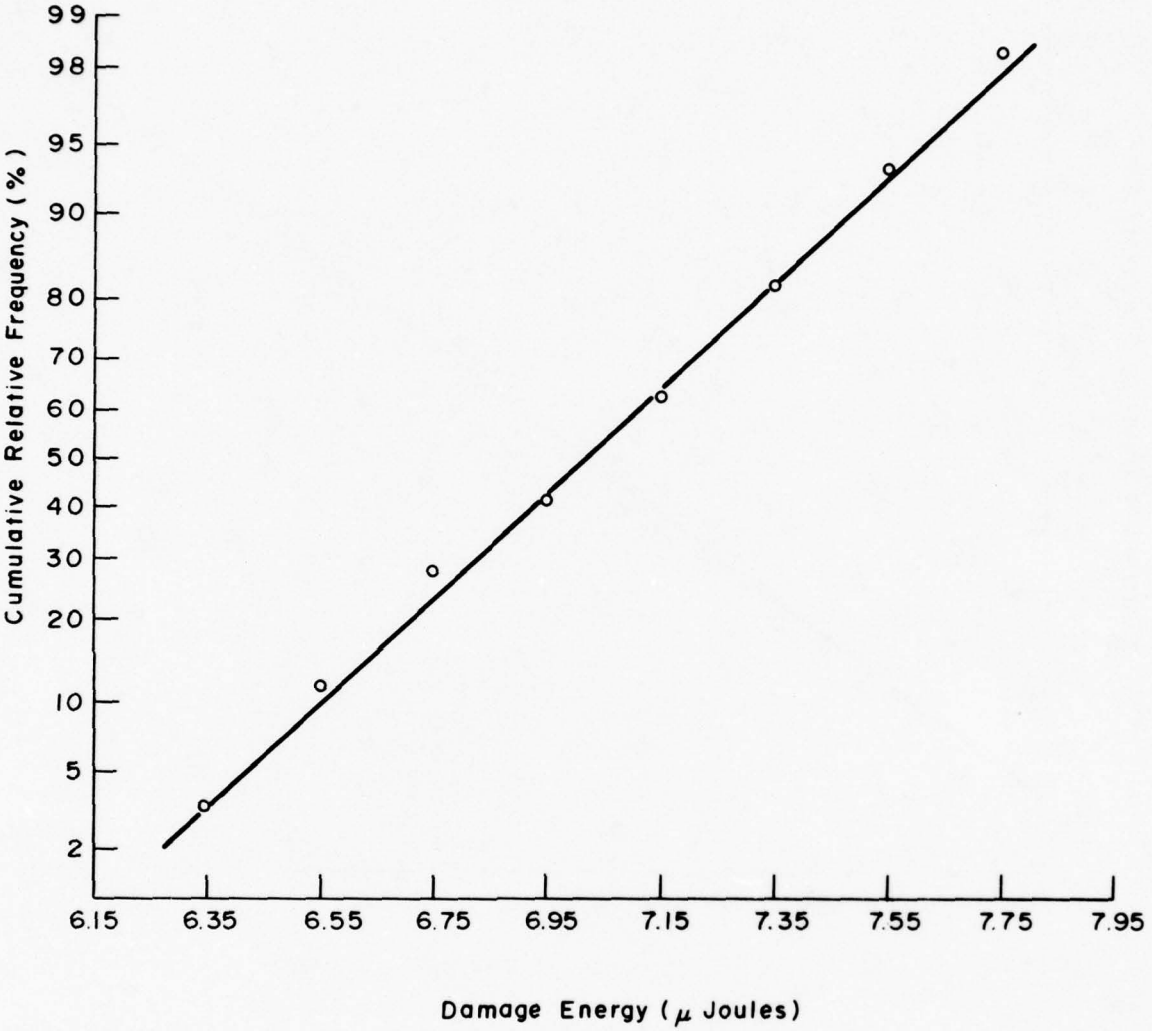

Fig. 7 JAN 2N918 DAMAGE ENERGY STATISTICS

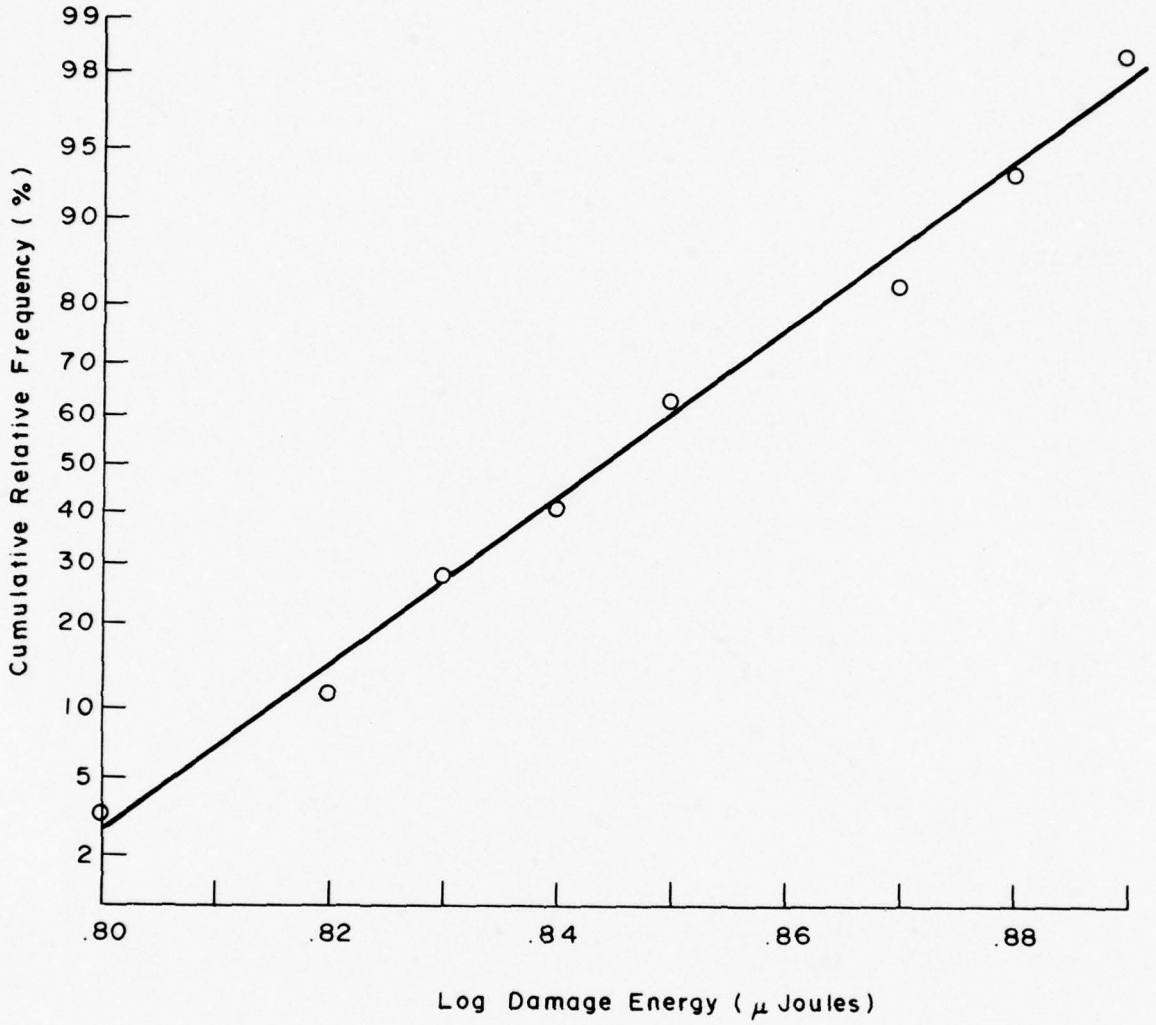

Fig. 8 JAN 2N918 DAMAGE ENERGY STATISTICS

A sample of 56 JANTX 1N914 diodes randomly chosen from the group purchased for the final life test were pulsed to destruction to determine the damage energy statistics. For the final life test, the method of pulsing the diodes was changed from that used during the preliminary tests to obtain better accuracy and control of the energy delivered to the 1N914's. It may be recalled that the first stress tests performed on the 1N914's used a 1 μsec pulse obtained by passing the output of a low power pulse generator through an Amplifier Research Model 1000L power amplifier. Due to the characteristics of the power amplifier it was very difficult to obtain accurately reproducible pulses. Due in part to the poor control of pulse energy, a resistor had to be placed in series with the diode being pulsed to assure that it would not burn out immediately at the onset of reverse breakdown due to the large amount of energy contained in the 1 μsec pulse at a reverse breakdown voltage of 120-180 volts. The power amplifier available did not allow the use of shorter pulses containing less energy.

To alleviate the above problems in diode pulsing, a constant current pulser, Rese Engineering Model 1051 Millimicrosecond Current Pulse Generator, was obtained. This unit, which produces a 0.1 μsec pulse, allowed the removal of the series resistor since the pulse current could be accurately controlled independently of the voltage thus limiting the energy delivered to the diode at the high reverse breakdown voltage. Data obtained with the 0.1 μsec pulse was scaled using the $t^{-\frac{1}{2}}$ damage model[7] to 1 μsec to assure that the damage constant is the same for both pulse widths and that the 0.1 μsec pulse is still sufficiently long to use the $t^{-\frac{1}{2}}$ model.

As in the preliminary tests the diodes were pulsed with the reverse biasing polarity and examined for changes in reverse leakage current after each pulse. The data thus obtained is tabulated in Appendix B. The mean damage energy based upon the 56 device samples was 53.11 μJoules comparing

closely with the published value of 54.8 μJoules. As with the transistors, the data may be partitioned into classes leading to a relative frequency histogram and finally a relative frequency distribution as shown in Figure 9. The distribution is clearly not normal since it is asymmetric and skewed to the right. When the cumulative relative frequency is plotted on a normal probability scale against the damage energy two straight lines are obtained as seen in Figure 10. This indicates that the low damage energy portion follows a normal distribution with mean 54.4 and standard deviation 11.4 while the high damage energy portion of the distribution is approximately normal with mean 56.5 and standard deviation 4.75. The significance of this result is unclear though it may mean that more than one damage mechanism is present.

3.3.3 EMP Stressing of Test Devices

Using the data obtained for the mean damage energies of the 2N918 and 1N914, the devices were stressed in preparation for the accelerated life test. Eighty-four (84) 2N918's were stressed at 0.93 mean damage energy (6.5 μJoules) and an equal number were stressed at 0.1 mean damage energy (0.7 μJoules). Five (5) pulses were applied to each device at the required stress level with sufficient time between pulses to allow return to ambient temperature. After each pulse the device was checked to assure that there was no performance degradation. Fourteen (14) 2N918's were damaged in obtaining the 84 pulsed to 0.93 mean damage energy while the distribution of Figure 6 predicts a loss of 9.58 devices. No transistors were damaged while pulsing at 0.1 mean damage energy.

Eighty-four (84) 1N914 diodes were stressed at 0.76 mean damage energy (40.4 μJoules). Again, five (5) pulses at the desired level were applied to each device during the stressing procedure. It should be noted that the diodes were stressed at a lower level than the transistors since the spread in the damage energy indicated that too many devices

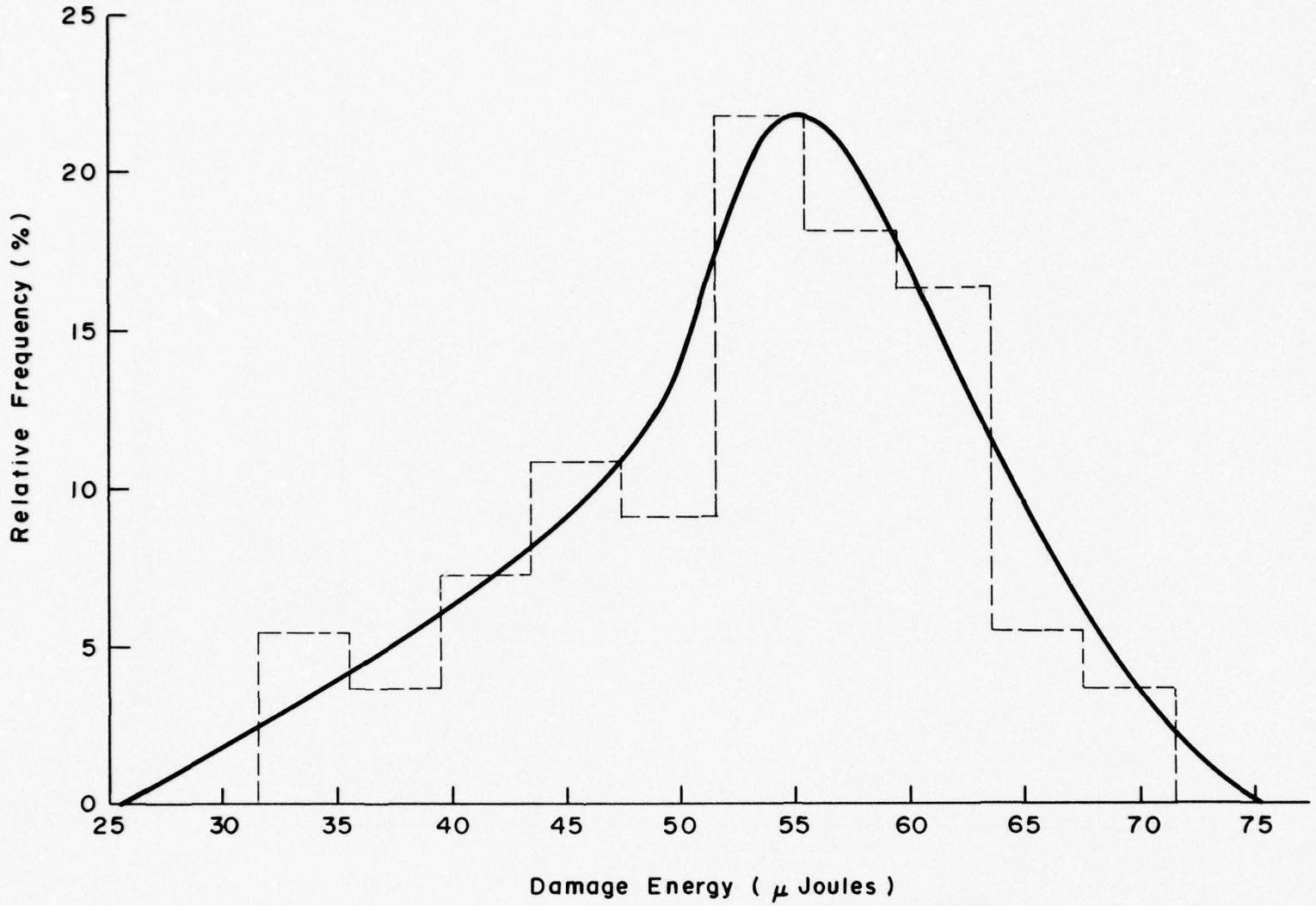

Fig. 9 JANTX IN914 DAMAGE ENERGY DISTRIBUTION

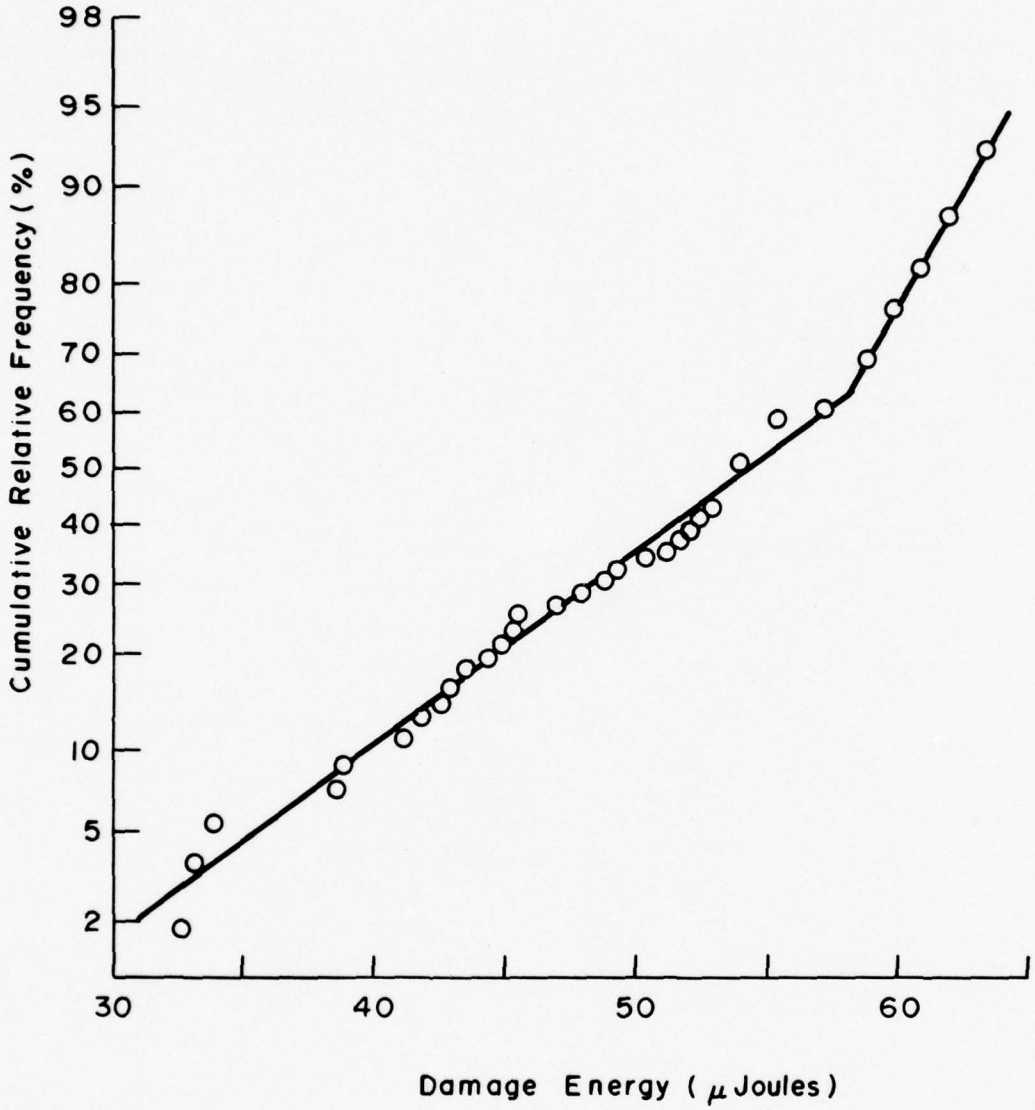

Fig. 10 JANTX IN914 DAMAGE ENERGY STATISTICS

would be destroyed if pulsed at 0.93 mean damage energy. Thirteen (13) diodes were destroyed while pulsing at 0.76 mean damage energy. The distribution of Figure 9 predicts a loss of 12 diodes under this condition. Two diodes were damaged at a stress of 0.1 mean damage energy and may be considered "freak" (abnormally weak) devices.

3.3.4 The Accelerated Life Test

The different groups of stressed and unstressed (i.e., the control groups) semiconductor devices were mounted on the test boards in an alternating pattern as illustrated below where S and L refer to devices stressed at the small and the large fraction of the damage energy and C refers to unstressed control devices.

L C S L C S
S L C S L C
C S L C S L
L C S L C S

The reason for this alternating array is to more evenly distribute the effects among all device groups should any section of the test boards suffer or cause wide spread or random failure or degradation. Each test board accomodates 64 devices distributed as above in an 8 row x 8 column format.

Before initiation of the life test, data was obtained on all of the test devices. The transistors were characterized by the measured value of h_{FE} while the diodes were characterized by the forward voltage for 10 mA forward current, the reverse breakdown voltage (reverse voltage for 100 μA reverse current), and the reverse leakage current at 20 and 80 volts reverse.

The 2N918's were biased to dissipate 114 mW and the 1N914's were biased to dissipate 167 mW corresponding to a chip temperature of 100°C based upon the manufacturer's thermal derating

data for these devices. The temperature of the junction was experimentally determined to assure that the use of the published thermal derating data was a valid approach.

For the JAN 2N918, junction temperature was measured by noting the variation of forward voltage across the emitter-base junction as a function of temperature for a constant current through the junction. Diode junction temperature was measured similarly by noting forward voltage as a function of temperature for a constant forward current. The resultant "thermometer curves" were obtained by placing the devices in an oven and making the required current and voltage measurements using short pulses having a low duty cycle to avoid heating the junction. Within experimental accuracy (approximately 10%), it was found that the junction temperature may be correctly determined as the sum of the ambient temperature and the chip temperature rise due to internal dissipation as calculated from the manufacturer's thermal resistance data.

With the junctions heated to 100°C by electrical dissipation, the oven was set to 200°C to obtain a total junction temperature of 300°C. At regular intervals throughout the test, h_{FE} was recorded for the transistors and the forward and reverse voltage-current characteristics were measured for the diodes. Since it was necessary to remove the devices from bias to make parameter measurements the junction temperature during the time data was being taken was approximately 200°C, the oven ambient. Data was recorded at the following time points:

16 hours	768 hours
168	840
336	936
456	1008
504	1128
600	1200
672	1282

Some difficulty was experienced in taking data with the devices at 200°C. This was especially troublesome in the case of the diodes. None of the reverse parameters, i.e., reverse breakdown and reverse leakage, could be reliably monitored due to the very large thermally induced leakage current. This current completely masked the desired parameters. However, the reverse voltage was recorded at 100 μA reverse current so that any change in the reverse behavior between data taking periods could be noted. If at the completion of the test program a diode was found to have failed in the reverse direction this data might help pinpoint the time of failure. The forward characteristics of the diodes could be measured without difficulty as could h_{FE} for the transistors.

4.0 RESULTS AND CONCLUSIONS

4.1 JAN 2N918 Bipolar Transistors - Results

The JAN 2N918's were operated at a junction temperature of 300°C for a total of 1282 hours. At the end of this period the test apparatus was returned to room temperature and h_{FE} was measured for all devices while on the test boards and again with the individual transistors removed from the test sockets and placed on a curve tracer. Some of the devices which showed degraded h_{FE} or complete failure when measured on the test board were found to be undamaged when removed from the board and tested with the curve tracer. This appeared to be due to leakage which developed in some defective test sockets. The staggered arrangement of the devices on the boards minimized the effect of the faulty sockets since the defective units were clustered. Hence approximately equal numbers of 0.93 stressed, 0.1 stressed, and control devices were effected. These devices (~ 5 from each group) were dropped from the test since it could not be determined whether or not the units were under full bias during portions of the life test.

Table 6 shows the number of JAN 2N918's failing in each group during the life test as a function of the chosen failure criterion. Since the group sizes are equal, it is immediately evident that for all definitions of failure considered there are significantly more failures (~ 10% higher) among the group stressed at 0.1 mean damage energy than among either the 0.93 stressed group or the control group. The devices stressed at 0.93 mean damage energy and the control group have a comparable number of failures.

TABLE 6

FAILURE CRITERIA

Failure Criterion	Failures at 0.93 Damage Energy	Failures at 0.1 Damage Energy	Failures in Control Group
Degradation of $h_{FE} \geq 20\%$	28	36	24
Degradation of $h_{FE} \geq 25\%$	20	29	22
Degradation of $h_{FE} \geq 35\%$	15	24	16
Degradation of $h_{FE} \geq 50\%$	12	19	14
Catastrophic Failure, $h_{FE} = 0$	9	19	14

Useful information on relative life and reliability may be obtained by plotting the cumulative percent failures within a group on a normal probability scale against the logarithm of the time to failure at 300°C. In constructing this graph, the failure criterion was chosen as a 20% or greater degradation in h_{FE}. The time to failure was obtained by examining the data on the failed devices taken at 200°C throughout the duration of the test. The time of failure was taken as the time at which the 200°C value of h_{FE} showed a significant drop. (It should be noted that the values of h_{FE} observed at 200°C are on the order of twice the room temperature values and the drop in h_{FE} at this temperature corresponding to a 20% drop at room temperature must be estimated.)

Figure 11 is the life distribution plot for the control and 0.93 stressed populations. For each group, the data fits a straight line indicating that the life distribution is lognormal. The lognormal life distribution is characteristic of thermally accelerated life test data as is consistent with the assumptions of the Arrhenius model.[2,3] The failure rate appears to be marginally higher among the 0.93 stressed population as indicated by the separation of the curves, but the difference is sufficiently small to be attributable to experimental error. The parallelism of the two straight lines is

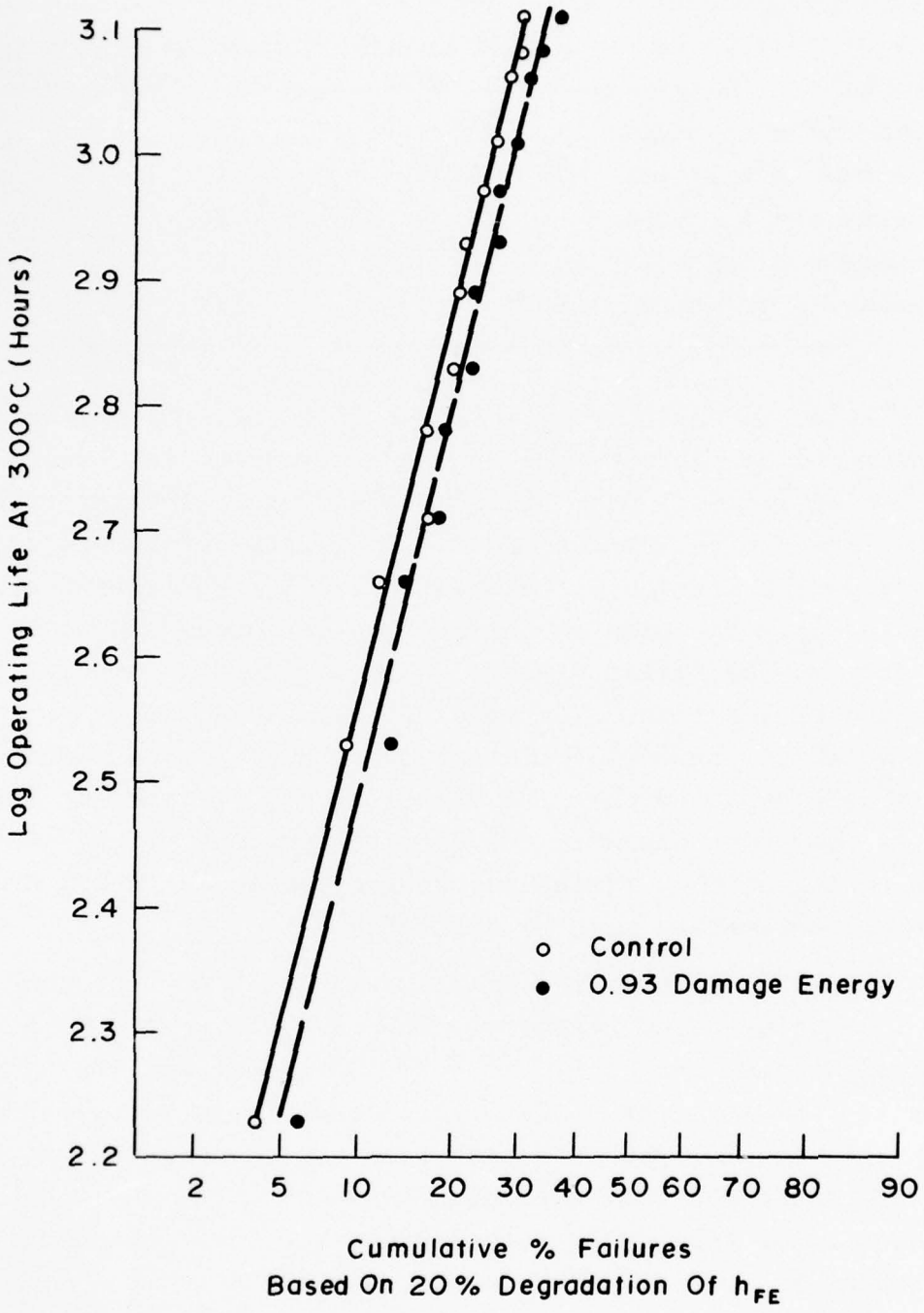

Fig. 11 JAN 2N918 LIFE BEHAVIOR

strongly indicative of a similar failure mechanism in both groups. If an activation energy of 1.02 eV is assumed (characteristic of Au-Al bond failures and surface inversion failures in silicon bipolar transistors[2]), the extrapolated median life from the Arrhenius relation is 1.82×10^8 hours at 100°C for the control group and 1.58×10^8 hours at 100°C for the 0.93 stressed group.

Figure 12 is the life distribution plot for the 0.1 stressed group and the control group. Unlike the control group and the 0.93 stressed group, the 0.1 stressed population is described by a broken line composed of two straight segments of different slope. This behavior indicates the presence of two different populations within the group with each having different life statistics. Such behavior might be expected if a different damage mechanism was present in some members of the group. The extrapolated median life for the population described by the line of smaller slope is 8.7×10^7 hours at 100°C. This differs by only a factor of two from the control group median life and is probably of little practical consequence in systems using a small number of devices since 8.7×10^7 hours represents almost 10^4 device years. Moreover, the life distribution of the 0.1 stressed population does not begin to deviate from the control until 500 operating hours have passed at 300°C. This corresponds to 3.2×10^7 hours at a nominal service temperature of 100°C.

4.2 JAN 2N918 Bipolar Transistor - Conclusions

The results obtained for the JAN 2N918 transistor are quite interesting when compared with the results which might have reasonably been expected. It is completely reasonable to expect that applying an EMP stress very near the threshold of damage may initiate some defect within the device. Initially, the induced weakness may not be observable as a change in an external parameter. However, with time and the accumulated stress of many operating hours in a service environment this

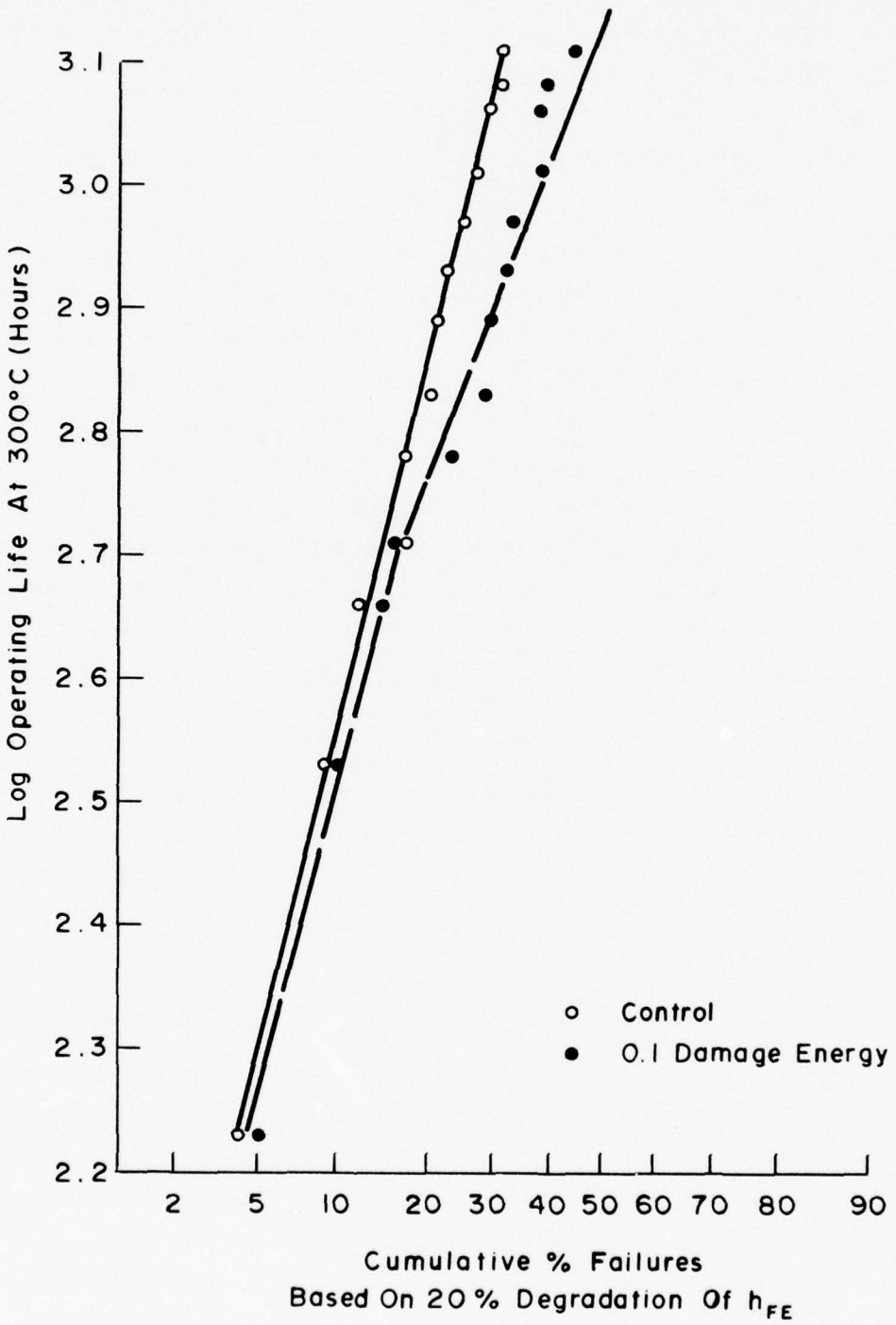

Fig. 12 JAN 2N918 LIFE BEHAVIOR

small defect may grow and finally cause the degradation of some vital operating parameter, thus leading to early failure. By the same logic, a very small applied EMP stress far below the damage threshold would not be expected to disrupt the device in any way since there is insufficient energy to initiate any damage mechanism. Hence most devices subject to such a stress should display normal life and reliability with the exception of that small population of devices having critical manufacturing defects.

The results obtained for the JAN 2N918 do not support the above argument. For all h_{FE} related damage criteria listed in Table 6, there are significantly more failures among the group of devices stressed at a small fraction of the damage threshold (0.1) than among either the unstressed control group or the heavily stressed (0.93 damage threshold) group. With this data it is possible to postulate a very different model for the effect of EMP stressing on this transistor.

Consider a transistor subjected to a pulse at a large fraction of the EMP damage threshold. If there are any slight flaws or defects present in the device which might cause current channeling through a small area of the device it will be degraded or destroyed by a pulse with sufficient energy. This may occur even though the level is somewhat below the damage threshold of a normal device. A device with no defects or irregularities which might promote current crowding and hot spot formation will safely withstand a high level pulse (below the damage threshold) with no observable damage to the device and, more importantly, with no hidden internal change or weakening of its material or structure. The only effect of this single high level pulse should be to heat the entire junction to within normal limits for the semiconductor material. By the above argument, if a group of 2N918's are subjected to a high but sub-damage threshold EMP stress, devices which are predisposed to failure due to internal weaknesses and flaws

will be promptly destroyed or damaged to such a degree that a parameter change may be readily observed. Devices which show no observable change will lead a normal life.

If the group of 2N918's above were stressed at a sufficiently small fraction of the damage threshold, those devices containing flaws would not be removed. The pulse energy might be insufficient to cause the defects present to worsen to the point where they are evidenced by prompt failure or parameter degradation. Although the low level pulse does not worsen the defect to the point where its effect is observable it may degrade it sufficiently to shorten the device life.

Consider as an example a faulty device in which an irregularity in the emitter metallization causes the current to concentrate at this point. Current through the junction will not be uniformly distributed but will be concentrated in a filament initiating at this irregularity. If a high level pulse is applied, enough energy flows through this channel to melt the silicon and cause abrupt failure. If a low level pulse is applied, there is insufficient energy to melt the silicon. However, the localized heating may well be sufficient to alter the local doping or perhaps melt some of the silicon proximal to the irregularity where the channel is most constricted without melting through the junction. Such an alteration of the material would not be observed externally but will lead to early failure under normal use.

It is important to stress that the results obtained for the JAN 2N918 may apply only to this particular device due to its structure. Moreover, the results may apply only to this particular production lot. Before these results may be generalized further work must be done both on the 2N918 and other device types. If the observations hold more generally they may be used to formulate an EMP test procedure. Devices to be screened should be tested at a large fraction of their EMP prompt damage threshold. Those devices which do not fail

and show no degradation will then survive a completely normal operating life. Screening at a low EMP stress level is contra-indicated since this appears to degrade long term reliability. While the degradation is unimportant in the time frame of normal system life (Figure 12 shows no appreciable difference in failure rate between the 0.1 stressed group and the control group until 3650 cumulative device years have passed at a service temperature of 100°C), it can become important in large high reliability systems containing hundreds or thousands of devices accumulating hundreds of thousands of device operating hours during a normal service life. An example of such systems is large communications networks.

4.3 JAN TX 1N914 Diodes - Results

At the completion of 1282 hours at 300°C the diodes were returned to room temperature and their forward and reverse characteristics measured for comparison to the pretest values. There was sufficient parameter change to indicate failure in only five devices. Two devices stressed at 0.1 mean damage energy failed as did two stressed at 0.76. One control device was judged to have failed. It is clear that there were insufficient failures to draw any conclusions about the effect of EMP stressing on the diodes.

It may be noted that there was indication of EMP stress related failures in the JAN TX 1N914 preliminary step stress test. These devices were purchased much earlier than those used in the final test and may well have been made with a different process. On April 2, 1976, Texas Instruments was granted approval for a construction change on the JAN TX 1N914 diode. This change consisted of substitution of a metallurgically bonded contact system for the previously used thermo compression contact system. Difficulties had been observed with the integrity of the anode and cathode chip metallization bond to the package plugs. Diodes mounted on circuit boards tended to exhibit abrupt forward voltage increase with gradual ambient

temperature change. It is believed that this mode of failure was observed in the batch of devices used for the step stress test and was absent in the final stress test. To obtain results for the present sample of diodes would require a much longer operating time or a higher operating temperature to compensate for the high damage mechanism activation energy normally observed for diodes.

5.0 RECOMMENDATIONS

IIT Research Institute believes that the results obtained from the accelerated life testing of the JAN 2N918 bipolar transistor are of sufficient potential importance to warrant further efforts in this area. The tests performed on the JAN 2N918 should be repeated with larger sample sizes and with the addition of an intermediate stress level of perhaps 0.5 mean damage energy. This might help determine more accurately at what stress level devices with the postulated internal weaknesses are screened out. In addition, larger samples and more time should be alloted to the step stress test to obtain the true activation energy and accelerating factors. A complete physics of failure analysis should be conducted to determine the predominant cause of failure in the stressed and control groups to see if any differences exist. This task may prove very difficult as previous attempts to locate the damage sites in extensively damaged, EMP stressed 2N918 transistors met with failure.[10]

If the results of this study are reproduced then similar studies should be carried out for devices of different internal geometry and different EMP sensitivity. This would indicate to what extent the results obtained for the JAN 2N918 are applicable to the class of silicon bipolar transistors as a whole and might lead to the formulation of a useful EMP screening procedure for such devices.

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APPENDIX A

THE ACCELERATED LIFE TEST APPARATUS

Accelerated life testing to achieve the goals of this program poses the following basic equipment requirements:

1. Heat resistant test circuit boards to hold the devices under test.
2. Circuitry to bias the devices under test.
3. A switching scheme to select one of two conditions, device under bias or device under measurement.
4. A switching scheme to allow monitoring the parameters of a selected device.
5. A temperature controlled oven to allow maintenance of the desired stressing temperature.

Two types of test boards were used in the accelerated life testing of the JAN 2N918 transistors and JAN TX 1N914 diodes. The transistors were mounted in special high temperature test sockets mounted with silver bearing eutectic solder to heat resistant printed circuit boards. The diodes were directly soldered to their test boards with eutectic solder. Both the transistors and diodes were arranged in 8 row by 8 column arrays (64 devices to a board) for compatibility with the parameter measurement selection matrix.

For the transistors, each emitter was tied to the base at the socket terminal through a 56 pf high temperature capacitor. This was done to inhibit parasitic oscillations. Individual teflon insulated wire leads were brought off the test boards for each emitter, base, and collector. The 64 emitter leads from each board were divided into two sets of 32 which were terminated in multipin connectors. The same arrangement was followed with the collector and base leads. The multipin connectors allowed the transistors to be connected either to bias sockets on the test

console or to sockets connected to the test selection matrix for parameter measurement. In the bias position, the collectors were connected to a positive bias supply and each emitter was grounded through an 80.6 ohm precision emitter resistor. Bias to all transistor bases was provided by a well regulated power supply from base to ground. A diode was placed in each base lead to protect the system from bias variations in the event of device failures due to junction short circuits.

The diode anodes were brought off the test boards and grouped in sets of 32, terminated in a multipin connector as with the transistors. The cathodes were all connected to common ground. With the multipin connectors in the bias position, bias was applied to each diode through a 10 ohm precision resistor.

With the multipin connectors connected to the test sockets on the test console, any one of the 64 devices on a test board could be accessed for measurement by a transistor curve tracer via a one out of 64 selection matrix using logic circuitry to control mercury wetted relays. The test selection matrix was designed in such a way that it could be readily interfaced with a Nova 1220 minicomputer for automatic data retrieval.

The four diode and four transistor test boards were mounted in an oven whose temperature could be held to within $\pm$ 2^{o}C. Temperature was monitored throughout the test with an iron-constantan thermocouple.

APPENDIX B

EMP DAMAGE THRESHOLD DATA

1.0 JAN 2N918 BIPOLAR TRANSISTOR

Texas Instruments Date Code/Lot No. 7643A.

Device Number	Damage Current (Amps)	Damage Voltage (Volts)	Damage Energy (μJoules)
A1	0.526	13.8	7.26
A11	0.526	13.8	7.26
A12	0.538	13.8	7.42
A13	0.538	14.1	7.58
A14	0.538	14.1	7.58
A15	0.515	13.5	6.97
A16	0.492	13.2	6.49
A17	0.538	14.7	7.90
A18	0.526	14.3	7.53
A19	0.481	13.3	6.39
A20	0.515	13.7	7.05
1	0.520	13.8	7.18
2	0.500	13.6	6.80
3	0.510	13.9	7.09
4	0.500	14.2	7.10
5	0.490	13.6	6.66
6	0.480	13.2	6.34
7	0.515	13.9	7.16
8	0.525	13.9	7.30
9	0.495	13.2	6.53
10	0.520	13.8	7.18
11	0.520	13.9	7.23
12	0.510	13.9	7.09
13	0.525	14.0	7.35
14	0.515	13.8	7.11
15	0.500	14.0	7.00
16	0.515	13.8	7.11
17	0.520	14.4	7.49

Device Number	Damage Current (Amps)	Damage Voltage (Volts)	Damage Energy (μJoules)
18	0.530	14.0	7.42
19	0.510	13.6	6.94
20	0.485	13.2	6.40
21	0.500	13.5	6.75
22	0.500	13.2	6.60
23	0.485	13.2	6.40
24	0.500	13.6	6.80
25	0.495	13.6	6.73
26	0.500	13.4	6.70
27	0.500	13.4	6.70
28	0.510	13.7	6.99
29	0.525	14.0	7.35
30	0.520	14.0	7.28
31	0.495	13.3	6.58
32	0.510	13.5	6.88
33	0.510	13.7	6.99
34	0.480	13.1	6.29
35	0.520	13.9	7.23
36	0.500	13.4	6.70
37	0.505	14.3	7.22
38	0.510	13.8	7.04
39	0.510	13.4	6.83
40	0.485	13.8	6.69
41	0.520	13.8	7.18
42	0.495	13.5	6.68
43	0.515	13.6	7.00
44	0.500	13.4	6.70
45	0.500	13.6	6.80
46	0.530	14.4	7.63
47	0.520	13.9	7.23
48	0.500	14.0	7.00
49	0.520	14.2	7.38
50	0.510	13.6	6.94

2.0 JAN TX 1N914 DIODE

Texas Instruments Date Code/Lot No. 7614.

Device Number	Damage Current (Amps)	Damage Voltage (Volts)	Damage Energy (μJoules)
A1	2.95	180	53.1
7/20A	2.00	170	34.0
7/20B	4.50	145	32.6
7/20B held the pulse for 50 nsec			
7/20C	2.65	200	53.0
A2	2.90	170	49.3
A3	3.45	180	62.1
A4	3.40	145	49.3
A5	2.10	185	38.8
A6	2.15	180	38.7
A7	3.80	167	63.4
A8	3.90	175	68.2
A9	2.90	185	53.6
A10	4.00	147	58.8
A11	2.75	162	44.5
A12	3.35	182	60.9
A13	2.80	162	45.4
A14	3.00	180	54.0
A15	3.00	185	55.5
A16	2.35	175	41.1
A17	2.72	160	43.5
A18	3.60	165	59.4
A20			55.1
A21			51.8
A22			53.2
A23			42.6
A24			59.4
A25			62.9
A26			44.4
A27			48.0
A28			60.9

Device Number	Damage Current (Amps)	Damage Voltage (Volts)	Damage Energy (μJoules)
A29			57.8
A30			42.9
A31			45.6
A32			61.0
A33			59.3
A34			53.4
A35			67.4
A37			59.0
A38			67.7
A39			50.4
A40			52.2
A41			41.9
A42			55.0
A43			63.5
A44			61.9
A45			63.8
A46			57.6
A47			61.9
A48			58.1
A49			51.4
A50			52.6
A51			47.0
A52			55.1
A55			57.2
A57			60.0
A58			33.2

APPENDIX C

GOODNESS OF FIT ANALYSIS FOR JAN 2N918 DAMAGE STATISTICS

The damage energy for the JAN 2N918 transistors was found to be distributed in an approximately normal manner. The degree to which the distribution approaches a normal distribution may be judged by the degree to which the plot of Figure 7 approaches a straight line. To obtain a better measure of the deviation of the observed distribution from normal, an analytical measure of the "goodness of fit" may be made.

The statistical test which has been applied to the distribution of Figure 6 is the chi-square test for goodness of fit. A measure of the difference between the observed distribution and a theoretical distribution is given by the statistic χ^2 given by:

$$\chi^2 = \sum_{j=1}^{k} \frac{(o_j - e_j)^2}{e_j} \qquad \text{(C-1)}$$

where o_j is an observed frequency and e_j is the frequency predicted by the theoretical distribution function.[18] If $\chi^2 = 0$ the observed and theoretical frequencies are in exact agreement. The larger the value of χ^2 the greater the difference between the observed and theoretical frequencies.

The sampling distribution of χ^2 is approximated by the chi-square distribution

$$Y = Y_o \, \chi^{\nu-2} \, e^{-\frac{1}{2}\chi^2} \qquad \text{(C-2)}$$

which is extensively tabulated in statistics references. In Equation (C-2) Y_o is a constant and ν is the number of degrees of freedom.

In practice, the value of χ^2 is computed by Equation (C-1) using the theoretical distribution and the data to obtain e_j and o_j respectively. The value of χ^2 thus obtained is then compared

with the value obtained from the sampling distribution Equation (C-2) for some critical value such as $\chi^2_{.95}$ [the value of χ^2 for which 5% of the area lies in the right hand tail of the distribution Equation (C-2)].

TABLE C-1

VALUES FOR COMPUTATION OF χ^2

Class Boundaries (μJoules)	Frequency Calculated From Normal Distribution	Observed Frequency
6.15		
	1.67	2
6.35		
	4.27	5
6.55		
	8.20	10
6.75		
	11.86	8
6.95		
	12.91	13
7.15		
	10.57	12
7.35		
	6.51	7
7.55		
	3.01	3
7.75		
	1.06	1
7.95		

The first column of Table C-1 lists the class boundaries used to partition the observed damage data into classes. The second column lists the number of devices in each class as predicted by the normal distribution of mean 7.01 μJoules and standard deviation 0.37 μJoules. The third column lists the number of devices actually observed in each class. Placing these values in Equation (C-1) yields

$$\chi^2 = 2.084$$

$\chi^2_{.95}$ obtained from the tables of the chi-square distribution for $\nu = 6$ (corresponding to nine classes) is 12.6. Since $2.084 < \chi^2_{.95}$ the data is an excellent fit to a normal curve of mean 7.01 μJoules and standard deviation 0.37 μJoules at the 95% confidence level. Comparison is also made with $\chi^2_{.05}$ to insure that the fit is not so good as to be unbelievable since one would not expect χ^2 to be too close to zero for any experimentally observed distribution. It is found that $\chi^2_{.05} = 1.64$. Since $2.084 > \chi^2_{.05}$ the fit is excellent but not unbelievably so.

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ATTN: DRDMI-EAA
ATTN: DRCPM-PE-EA, W. Wagner
ATTN: DRCPM-PE-EG, W. Johnson

U.S. Army Test and Evaluation Comd.
ATTN: DRSTE-FA

U.S. Army Training and Doctrine Comd.
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White Sands Missile Range
ATTN: STEWS-TE-AN, J. Okuma

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Naval Construction Battalion Center
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Naval Ship Engineering Center
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Naval Surface Weapons Center
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ATTN: Code WR43, L. Libelo
ATTN: Code F-30

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Strategic Systems Project Office
ATTN: NSP-43
ATTN: NSP-2701, J. Pitsenberger

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ATTN: SUL
ATTN: ELP, W. Page
ATTN: ELXT
ATTN: NT
ATTN: CA
ATTN: ELA, J. Castillo
ATTN: ELP

Air University
ATTN: AUL/LSE-70-250

Electronic Systems Division/YSEA
ATTN: YSEA

Foreign Technology Division, AFSC
ATTN: ETDP, B. Ballard

Ogden ALC/MMEDDE
ATTN: OO-ALC/MMETH, P. Berthel
ATTN: MMEDO, L. Kidman
ATTN: R. Blackburn

Rome Air Development Center, AFSC
ATTN: TSLD

Space & Missile Systems Organization/IN
Air Force Systems Command
ATTN: IND

Space & Missile Systems Organization/MN
Air Force Systems Command
ATTN: MNNH, M. Baran
ATTN: MNNH, R. Lawrence

Space & Missile Systems Organization/YA
Air Force Systems Command
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Strategic Air Command/XPFS
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ATTN: SPFS, B. Stephan
ATTN: G. Matzke
ATTN: NRI-STINFO, Library

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Lawrence Livermore Laboratory
ATTN: Doc. Con. for L-96, H. Kruger
ATTN: Doc. Con. for L-96, T. Donich
ATTN: Doc. Con. for Technical Information Department

Los Alamos Scientific Laboratory
ATTN: Doc. Con. for C. Benton

Sandia Laboratories
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Department of the Interior
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Department of Transportation
Federal Aviation Administration
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General Electric Co.-TEMPO
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ATTN: DASIAC
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Georgia Institute of Technology
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Grumman Aerospace Corp.
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GTE Sylvania, Inc.
Electronics Systems Grp. - Eastern Div.
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GTE Sylvania, Inc.
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Honeywell, Inc.
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Institute for Defense Analyses
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International Tel. & Telegraph Corp.
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JAYCOR
Santa Barbara Facility
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JAYCOR
ATTN: R. Stahl/E. Wenaas

JAYCOR
ATTN: Library

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Data Systems Division
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ATTN: EMC GP

Litton Systems, Inc.
AMECOM Division
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Lockheed Missiles & Space Co., Inc.
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Lockheed Missiles & Space Co., Inc.
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McDonnell Douglas Corp.
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Mission Research Corp.
EM System Applications Division
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Mission Research Corp.-San Diego
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Mitre Corp.
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Northrop Research and Technology Ctr.
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Raytheon Co.
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Raytheon Co.
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RCA Corp.
Camden Complex
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Rockwell International Corp.
Space Division
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Rockwell International Corp.
ATTN: Technical Information Center

Rockwell International Corp.
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Science Applications, Inc.
ATTN: F. Tesche

Science Applications, Inc.
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Science Applications, Inc.
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Sidney Frankel & Associates
ATTN: S. Frankel

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Sperry Division
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Sperry Rand Corp.
Sperry Flight Systems
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SRI International
ATTN: A. Whitson

SRI International
ATTN: M. Hullings

Texas Instruments, Inc.
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